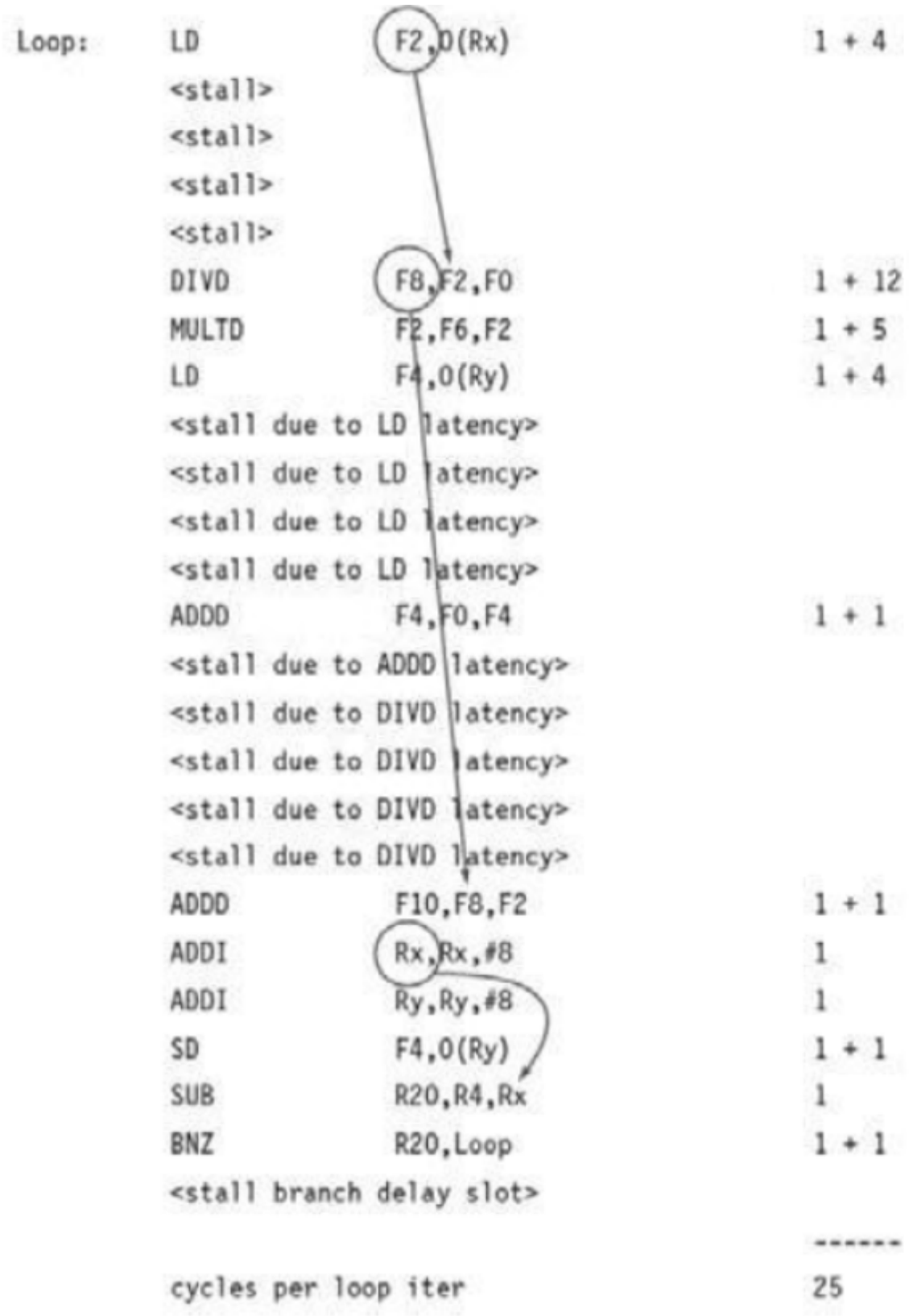
3.1

Loop:	LD	F2,0(Rx)	1 + 4
	DIVD	F8,F2,F0	1 + 12
	MULTD	F2,F6,F2	1 + 5
	LD	F4,0(Ry)	1 + 4
	ADDD	F4,F0,F4	1 + 1
	ADDD	F10,F8,F2	1 + 1
	ADDI	Rx,Rx,#8	1
	ADDI	Ry,Ry,#8	1
	SD	F4,0(Ry)	1 + 1
	SUB	R20,R4,Rx	1
	BNZ	R20,Loop	1 + 1
			———
		cycles per loop iter	40

3.2


Loop: LD F2,0(Rx) 1 + 4
<stall>
<stall>
<stall>
<stall>
DIVD F8,F2,F0 1 + 12
MULTD F2,F6,F2 1 + 5
LD F4,0(Ry) 1 + 4
<stall due to LD latency>
<stall due to LD latency>
<stall due to LD latency>
<stall due to LD latency>
ADDD F4,F0,F4 1 + 1
<stall due to ADDD latency>
<stall due to DIVD latency>
<stall due to DIVD latency>
<stall due to DIVD latency>
<stall due to DIVD latency>
ADDD F10,F8,F2 1 + 1
ADDI Rx,Rx,#8 1
ADDI Ry,Ry,#8 1
SD F4,0(Ry) 1 + 1
SUB R20,R4,Rx 1
BNZ R20,Loop 1 + 1
<stall branch delay slot>
cycles per loop iter 25

3.3

	Execution pipe 0		Execution pipe 1
Loop:	LD F2,0(Rx)	;	<nop>
	<stall for LD latency>	;	<nop>
	<stall for LD latency>	;	<nop>
	<stall for LD latency>	;	<nop>
	<stall for LD latency>	;	<nop>
	DIVD F8,F2,F0	;	MULTD F2,F6,F2
	LD F4,0(Ry)	;	<nop>
	<stall for LD latency>	;	<nop>
	<stall for LD latency>	;	<nop>
	<stall for LD latency>	;	<nop>
	<stall for LD latency>	;	<nop>
	ADD F4,F0,F4	;	<nop>
	<stall due to DIVD latency>	;	<nop>
	<stall due to DIVD latency>	;	<nop>
	<stall due to DIVD latency>	;	<nop>
	<stall due to DIVD latency>	;	<nop>
	<stall due to DIVD latency>	;	<nop>
	<stall due to DIVD latency>	;	<nop>
	ADDD F10,F8,F2	;	ADDI Rx,Rx,#8
	ADDI Ry,Ry,#8	;	SD F4,0(Ry)
	SUB R20,R4,Rx	;	BNZ R20,Loop
	<nop>	;	<stall due to BNZ>
	cycles per loop iter 22		

3.9

```
addi T0, x1, x1
addi T1, T0, T0
addi x1, T1, T1
```

Value in X1 should be 40

3.15

a.

Iteration	Instruction	Issues at	Executes/memory	Write CDB at	Comment
1	fld F2,0(x1)	1	2	3	First issue
1	fmul.d F4,F2,F0	2	4	19	Wait for F2 Mult rs [3–4] Mult use [5–18]
1	fld F6,0(x2)	3	4	5	Ldbuf [4]
1	fadd.d F6,F4,F6	4	20	30	Wait for F4 Add rs [5–20] Add use [21–29]
1	fsd F6,0(x2)	5	31		Wait for F6 Stbuf1 [6–31]
1	addi x1,x1,#8	6	7	8	
1	addi x2,x2,#8	7	8	9	
1	sltu x3,x1,x4	8	9	10	
1	bnez x3,foo	9	11		Wait for x3
2	fld F2,0(x1)	10	12	13	Wait for bnez Ldbuf [11–12]
2	fmul.d F4,F2,F0	11	14 19	34	Wait for F2 Mult busy Mult rs [12–19] Mult use [20–33]
2	fld F6,0(x2)	12	13	14	Ldbuf [13]
2	fadd.d F6,F4,F6	13	35	45	Wait for F4 Add rs [14–35] Add use [36–44]
2	fsd F6,0(x2)	14	46		Wait for F6 Stbuf [15–46]
2	addi x1,x1,#8	15	16	17	
2	addi x2,x2,#8	16	17	18	
2	sltu x3,x1,x4	17	18	20	
2	bnez x3,foo	18	20		Wait for x3
3	fld F2,0(x1)	19	21	22	Wait for bnez Ldbuf [20–21]
3	fmul.d F4,F2,F0	20	23 34	49	Wait for F2 Mult busy Mult rs [21–34] Mult use [35–48]
3	fld F6,0(x2)	21	22	23	Ldbuf [22]
3	fadd.d F6,F4,F6	22	50	60	Wait for F4 Add rs [23–49] Add use [51–59]
3	fsd F6,0(x2)	23	55		Wait for F6 Stbuf [24–55]
3	addi x1,x1,#8	24	25	26	
3	addi x2,x2,#8	25	26	27	
3	sltu x3,x1,x4	26	27	28	
3	bnez x3,foo	27	29		Wait for x3

b.

Iteration	Instruction	Issues at	Executes/memory	Write CDB at	Comment
1	fld F2,0(x1)	1	2	3	
1	fmul.d F4,F2,F0	1	4	19	Wait for F2 Mult rs [2–4] Mult use [5]
1	fld F6,0(x2)	2	3	4	Ldbuf [3]
1	fadd.d F6,F4,F6	2	20	30	Wait for F4 Add rs [3–20] Add use [21]
1	fsd F6,0(x2)	3	31		Wait for F6 Stbuf [4–31]
1	addi x1,x1,#8	3	4	5	
1	addi x2,x2,#8	4	5	6	
1	sltu x3,x1,x4	4	6	7	INT busy INT rs [5–6]
1	bnez x3,foo	5	7		INT busy INT rs [6–7]
2	fld F2,0(x1)	6	8	9	Wait for BEQZ
2	fmul.d F4,F2,F0	6	10	25	Wait for F2 Mult rs [7–10] Mult use [11]
2	fld F6,0(x2)	7	9	10	INT busy INT rs [8–9]
2	fadd.d F6,F4,F6	7	26	36	Wait for F4 Add xS [8–26] Add use [27]
2	fsd F6,0(x2)	8	37		Wait for F6
2	addi x1,x1,#8	8	10	11	INT busy INT rs [8–10]
2	addi x2,x2,#8	9	11	12	INT busy INT rs [10–11]
2	sltu x3,x1,x4	9	12	13	INT busy INT rs [10–12]
2	bnez x3,foo	10	14		Wait for x3
3	fld F2,0(x1)	11	15	16	Wait for bnez
3	fmul.d F4,F2,F0	11	17	32	Wait for F2 Mult rs [12–17] Mult use [17]
3	fld F6,0(x2)	12	16	17	INT busy INT rs [13–16]
3	fadd.d F6,F4,F6	12	33	43	Wait for F4 Add rs [13–33] Add use [33]
3	fsd F6,0(x2)	14	44		Wait for F6 INT rs full in 15
3	addi x1,x1,#8	15	17		INT rs full and busy INT rs [17]
3	addi x2,x2,#8	16	18		INT rs full and busy INT rs [18]
3	sltu x3,x1,x4	20	21		INT rs full
3	bnez x3,foo	21	22		INT rs full

3.16

Instruction	Issues at	Executes/memory	Write CDB at
fadd.d F2,F4,F6	1	2	12
add x1,x1,x2	2	3	4
add x1,x1,x2	3	5	6
add x1,x1,x2	4	7	8
add x1,x1,x2	5	9	10
add x1,x1,x2	6	11	12 (CDB conflict)

3.17

(a)

Branch PC mod 4	Entry	Prediction	Outcome	Miss	Update
2	4	T	T	NO	X
3	6	NT	NT	NO	NT
1	3	T	NT	YES	T with one miss
3	7	NT	NT	NO	X
1	3	T	NT	YES	NT
2	5	T	T	NO	X
1	2	NT	NT	NO	X
2	5	T	T	NO	X
3	6	NT	T	YES	NT with one miss

Miss rate = 3/9 = 1/3

(b)

Branch PC mod 4	Entry	Prediction	Outcome	Miss	Update
0	0	T	T	NO	T
1	4	T	NT	YES	T with one miss
1	5	T	NT	YES	NT
1	7	NT	NT	NO	X
1	7	NT	NT	NO	X
0	0	T	T	NO	X
1	7	NT	NT	NO	X
0	0	T	T	NO	X
1	7	NT	T	YES	NT with one miss

Miss rate = 3/9

3.18

$$\text{Speedup} = \frac{\text{CPI}_{\text{noBTB}}}{\text{CPI}_{\text{BTB}}} = \frac{\text{CPI}_{\text{base}} + \text{Stalls}_{\text{base}}}{\text{CPI}_{\text{base}} + \text{Stalls}_{\text{BTB}}}$$

$$\text{Stalls}_{\text{noBTB}} = 15\% \times 2 = 0.30$$

To compute $\text{Stalls}_{\text{BTB}}$, consider the following table:

BTB result	BTB prediction	Frequency (per instruction)	Penalty (cycles)
Miss		$15\% \times 10\% = 1.5\%$	3
Hit	Correct	$15\% \times 90\% \times 90\% = 12.1\%$	0
Hit	Incorrect	$15\% \times 90\% \times 10\% = 1.3\%$	4

Therefore:

$$\text{Stalls}_{\text{BTB}} = (1.5\% \times 3) + (12.1\% \times 0) + (1.3\% \times 4) = 0.097$$

$$\text{Speed up} = \frac{1.0 + 0.30}{1.0 + 0.097} = 1.2$$