In this homework, represent your IP in synthesizable HDL. Make sure that your IP is AMBA-compliant.

You have to take the following considerations into account:

- Pass the following Rule Checking of HDL coding conventions. Explain the reasons of any violation.
  
  **Coding conventions:**
  - Best Practices
  - OpenMORE
  - DFT
  - RMM
  - FPGA
  - Synth (rules related to logic synthesis)

- Both **statement** and **Branch** Metrics of all the sub-modules of your IP must be 100% (exclude your testbench). If not, please explain the reasons.

- Separate your IP kernel and AHB bus interface into different modules and design files. Examples for AHB bus interface can be found in Install\Logic Modules\LM-XCV600E\ (e.g., C:\Program Files\ARM\Logic Modules\LM-XCV600E\) of PC.

The following documents can be found in **SVNAVIGATOR/help/pdfs/** (e.g., /RAID/EDA/VN/help). If you write your design in VHDL, you have better read the relative documents.

- VN-Check User Guide, 2002.05.02.01
- VN-Cover User Guide, 2002.05.01.01
- Verification Navigator User Guide, 2002.05.00.01
- Verilog rules supplied with VN-Check, version 2002.05
- VHDL rules supplied with VN-Check, version 2002.05


Deliverable

Your deliverable has to include:
1. Report that describes your idea and result. Also, your report has to include the following “Sections”
   - Architecture of your IP:
     I. Describe the architecture and control scheme (page 124, chapter 3 of handout) of your IP.
     II. Draw a block diagram of your IP such that each block corresponds to the sub-module of your HDL design.
   - Memory requirement:
     I. Describe the memory usage of your IP.
     II. If your IP requires a large memory, you have to incorporate a memory model, e.g., SSAM model, SDRAM model, embedded memory model.
   - Quality of your HDL code:
     I. List the results of the check of coding conventions and the coverage of statement and branch metrics in table format.
     II. Explain the reasons that the design does not satisfy the rules and coverage scores.
   - Features of your IP:
     I. Describe the flexibility of your IP, such as the parameterized design presented in page5-9, chapter 4 of handout.
     II. Describe the superior features of your IP compared to the off-the-shelf one.
   - Verification plan:
     I. Describe the ways you verify the features, flexibility and AHB-compliant interface of your IP.
2. Source code of your IP.
3. All setting and information required for regenerating the result shown in your report. If the results of the check of coding conventions and the coverage of statement and branch metrics can not be regenerated by using your information, the report will not be recognized.

Important Date

Due : 5:00 p.m. Wednesday, Dec. 18, 2002

For more information

- The contents of this document: Kun-Bin Lee
- ARM development tools: contact the TA with the number = your team number %4

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