DEE 5012 VLSI Signal Processing

Midterm Exam

2004/4/19 1:30~3:20pm

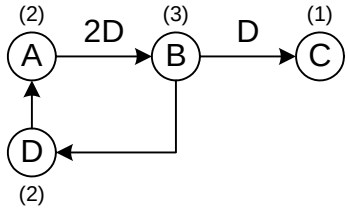
1. Basic Concepts (28 points)

(a) The following six terms are used to characterize a DSP architecture. Please describe the relationship and differences between them (10%)

Iteration period; Iteration bound; Sample period; Clock period; Critical path; Critical loop

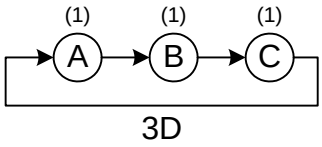
(b) How to improve a DSP architecture (represented in SDFG) with its iteration bound larger than the sample period? List two possible methods. (4%)

(c) Use the ***LPM*** method to determine the ***iteration bound*** of the following SDFG (10%)



(d) Explain why the complexity of a centralized register file grows as the cubic of the number of functional units (4%)

2. Retiming (16 points)



(a) What is the ***iteration bound***? (2%)

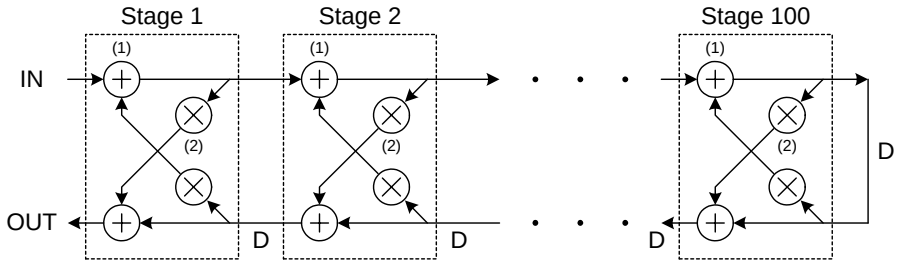
(b) What is the ***retiming space***? (3%)
(i.e. write down the feasibility constraints)

(c) Write down the ***W*** & ***D*** matrices by inspection. (6%)

(d) What are the ***critical-path constraints*** for critical path ≤ 1? (3%)

(e) Find a valid set of ***retiming values*** for critical path ≤ 1 (2%)

3. Retiming (12 points)



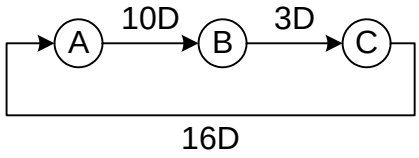
(a) Identify the ***critical path***. (2%) What is the ***minimum clock period***? (2%)

(b) Improve the design by retiming and identify the ***new critical path***. (4%) What is the ***minimum clock period*** now? (2%)

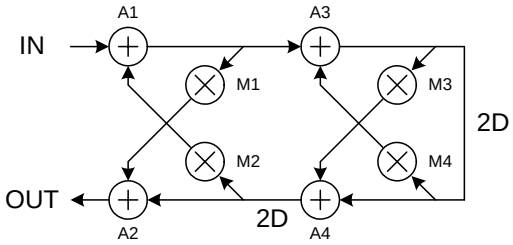
(c) What is the ***improvement ratio***? (2%)

4. Unfolding Transform (8 points)

Unfold the following SDFG by a factor of 4



5. Folding Transform (36 points)



(a) Draw the ***acyclic precedence graph*** and find the ***ASAP*** schedule (assume all functional units have single-cycle latency) (6%)

(b) Assume there exist only a multiplier and an adder, both of which have registered I/O ports (i.e. two-cycle latency, or $P_M = P_A = 2$). Find a ***schedule*** with the minimum cycles depending on (a). Use the index order (e.g. schedule A_i before A_j if $i < j$) if the resources conflict. (6%)

(c) Use the minimum cycles in (b) as the folding factor (i.e. non-overlapped iterations). Write down the ***folding equations***. (6%)

(d) Design the SIU-based architectures with (i) the ***output queue***, (ii) the ***input queue***, and (iii) the ***forward-backward register allocation***, depending on (c). (18%)