forcing $w_r(\hat{e}_i) \geq 0$ for $1 \leq i \leq k$. Therefore, $w_r(\hat{e}_i) = 0$ for at least 1 edge $\hat{e}_i$. Since the value of $w_r(p_i) = w_r(e_i) + w_r(\hat{e}_i) = w_{max} + r(\hat{U}) - r(U)$ is the same for $1 \leq i \leq k$, the edge e_j with $w_r(e_j) = w_{r,max}$ is in the path p_j which has $w_r(\hat{e}_j) = 0$. Thus, $w_r(e_j) = w_r(p_j) = w_{max} + r(\hat{U}) - r(U)$. ■

Details of Step 2: The cost of the edges in the fanout model is

$$\begin{aligned} COST &= \sum_{i=1}^{k} (w_r(e_i)\beta(e_i) + w_r(\hat{e}_i)\beta(\hat{e}_i)) \\ &= \frac{1}{k}\left(\sum_{i=1}^{k} (w_r(e_i) + w_r(\hat{e}_i))\right) \\ &= \frac{1}{k}(k)\left(w_{max} + r(\hat{U}) - r(U)\right). \blacksquare \end{aligned}$$

4.5 CONCLUSIONS

Synchronous systems can be retimed to reduce critical path or clock period, number of storage or delay elements, or power consumption. Shortest path algorithms can be used to obtain a retiming solution if one exists. All possible retiming solutions can also be obtained by *exhaustive retiming* using approaches in [5],[6]. Retiming can also be used as a preprocessing step for folding and for computation of roundoff noise as discussed in Chapters 6 and 11, respectively. Use of retiming for reduction of power consumption is covered in Section 17.5.4. Retiming of multirate DFGs is addressed in the context of multirate folding in Section 6.5. Retiming of 2D DFGs has been addressed in [7],[8].

4.6 PROBLEMS

1. Consider the wave digital filter shown in Fig. 4.15. Assume that each multiply operation requires 20 nsec and each add operation requires 8 nsec.

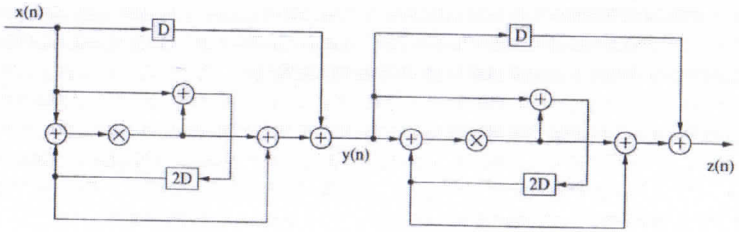

Fig. 4.15 The wave digital filter structure in Problem 1.

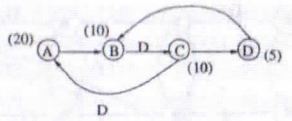

Fig. 4.16 Data-flow graph for Problem 2.

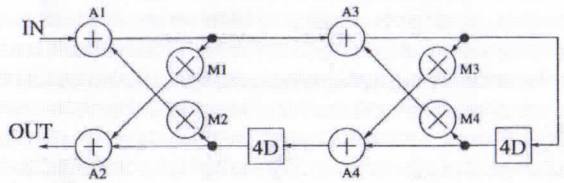

Fig. 4.17 A 4-level pipelined all-pass 8th-order IIR digital filter.

   (a) Calculate the iteration period bound of this filter by inspection.
   (b) What is the critical path?
   (c) Manually pipeline and/or retime this filter to achieve a critical path equal to the iteration period bound.

2. Consider the DFG shown in Fig. 4.16, where the number at each node denotes its execution time.
   (a) What is the maximum sample rate of this DFG?
   (b) What is the fundamental limit on the sample period for the system described by this DFG?
   (c) Manually retime this DFG to minimize the clock period.

3. Consider the 4-level pipelined all-pass 8th-order IIR digital filter DFG in Fig. 4.17. Assume that addition and multiplication require 1 and 2 u.t., respectively.
   (a) By inspection, calculate the iteration bound.
   (b) Compute the critical path time of the circuit.
   (c) Pipeline and/or retime this system to achieve a critical path of 2 u.t. Do this by inspection (manually).

4. Consider the 6th-order orthogonal filter structure shown in Fig. 4.18. All operations in this structure are CORDIC (coordinate rotation digital computer) rotation operations, which are orthonormal. Assume that each CORDIC rotation operation requires T nsec.

   What is the iteration bound of this filter? What is the critical path of this filter? Manually pipeline and/or retime the filter structure to