supply voltage of 5 V, at what level should the system be pipelined? What is the supply voltage of the pipelined system?

10. Two implementations of an 8-tap FIR filter are shown in Fig. 3.24. Assume the critical path (or the propagation delay) of a multiplier to

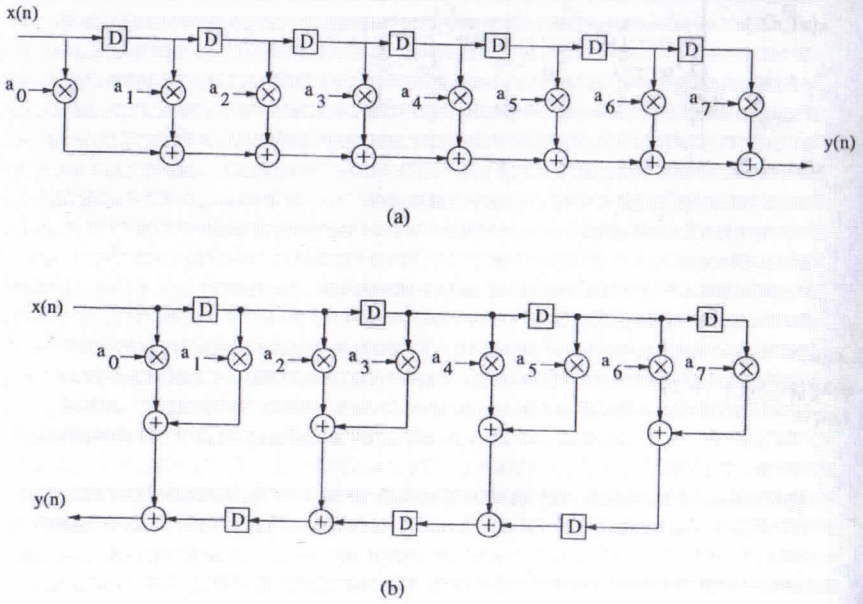

Fig. 3.24 Two implementations of an 8-tap FIR filter in Problem 10.

be twice that of an adder, i.e., $T_m = 2T_a$. Therefore, the charging capacitance of a multiplier is twice that of an adder. Further assume that the total capacitance of a multiplier is 10 times that of an adder, i.e., $C_m = 10C_a$. The critical path of the direct-form structure in Fig. 3.24(a) is $T_m + 7T_a = 9T_a$. The structure in Fig. 3.24(b) can be operated with a lower supply voltage to meet the clock period or sampling period constraint of $9T_a$. Thus, the structure in Fig. 3.24(b) can be used to reduce the power consumption. Assume that the structure in Fig. 3.24(a) is operated with a supply voltage of 4 V. Assume the technology threshold voltage to be 0.5 V. The supply voltage must be greater than 1.2 V to achieve the acceptable noise margin.

What is the minimum supply voltage at which the structure shown in Fig. 3.24(b) can be operated to achieve the desired sampling period of $9T_a$? Calculate the percentage of reduction in power consumption for the structure in Fig. 3.24(b) as compared with that in Fig. 3.24(a). Neglect the propagation delay and capacitance of delay elements in calculation of critical path or power consumption.

11. Consider a datapath with a total capacitance of C_{total}. This datapath is pipelined by M levels. Let C_{latch} represent the total capacitance of the latches used for 1 pipelining stage. The pipelined system is operated with lower supply voltage to reduce the power consumption. Assume both systems are operated at same speed and assume the propagation delay of the latch to be negligible. Let $C_{total} = 10C_{latch}$, $V_{dd} = 4$ V and $V_t = 0.6$ V. Calculate the power consumption of the pipelined system as a percentage of that of the sequential system for different values of M. What is the optimal M for least power consumption?

12. Calculate the power reduction of a computation if it is pipelined by 4 stages and processed using a block structure with block size 4, but is operated with the same sample rate as the original system. Assume that the original system was operated at a supply voltage of 5 V, and assume the threshold voltage V_t of the CMOS process to be 0.4 V. Calculate the power consumption of the parallel-pipelined system as compared with the original system. What is the operating supply voltage of the parallel-pipelined system?

13. Consider an FIR digital filter operated with a clock or sample period T. This problem can be solved without knowing the order of the filter. The filter circuit is operated with a supply voltage of 5 V using a technology with threshold voltage of 0.4 V. The consumer demand imposes the constraint that the sample speed of the filter be increased by 4 times, i.e., the new system should achieve a sample period of $T/4$. In addition, the power should also be reduced, possibly at the expense of increasing the area. To reduce the power consumption, a lower supply voltage can be used. Assume the availability of a variable voltage supply that can generate voltages from 1.0 to 5 V. The supply voltage cannot be less than 1.0 V.

    The simultaneous speed increase and power reduction can be achieved by using block processing using block size that is a multiple of 4. For example, we can use a parallel FIR filter with block size 8 and operate this system with clock period $2T$ to achieve a sample period $T/4$. Similarly, we can use parallel filters with block size $4p$ and operate the filter with clock period pT to achieve sample period $T/4$ where p is any positive integer. These filters can then be operated with lower supply voltage to reduce power consumption.

    (a) What value of p or block size should be chosen to obtain a circuit with the least power consumption? Calculate the supply voltage and power consumption for this p.

    (b) If the goal is not to reduce the power, but to reduce the area-power product, what value of p or block size should be chosen? Calculate the supply voltage, power consumption, and area-power product