VLSI Signal Processing Systems

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Course Information

- Lecture:
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Course Information

- **Text**
  - Keshab K. Parhi, *VLSI Digital Signal Processing Systems – Design and Implementation*, Wiely, 1999
- **Project**
  - The project can be individual project or a group project
  - Project type can be either theory/algorithm development type or implementation type
  - Project report is required to be submitted before the end of this course
  - At the last week of this course, project presentation will take place in class
- **Course Grade**
  - Home work and project report (50%)
  - Midterm Exam. 25%
  - Final Exam. 25%

What is VSP?

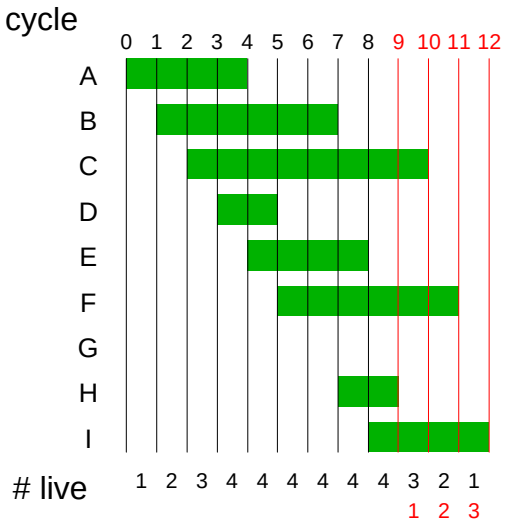
- This course will cover the most important methodologies for designing custom or semi-custom VLSI systems for some typical digital signal processing applications.
- In this course, you will learn how to map DSP algorithms into VLSI efficiently. Several high-level algorithm and architecture design techniques will be introduced that enable joint optimization across the algorithmic, architectural, and circuit domains

Data Format Converter

- e.g. 3-by-3 Matrix transposition
  input sequence: ABCDEFGHI
  output sequence: ADGBEHCFI

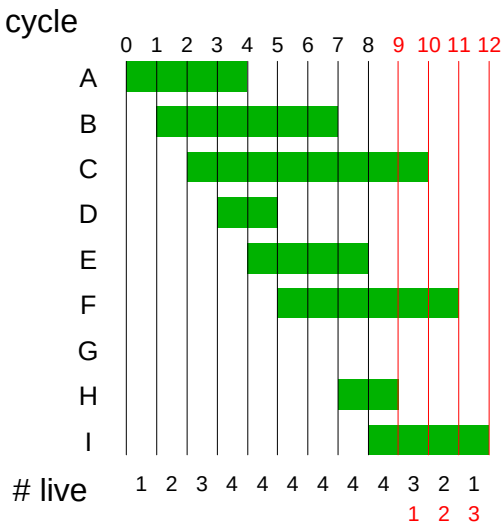
Step 1: Lifetime analysis

Sample	Tinput	Tzlout	Tdiff	Toutput	Life Period
A	0	0	0	4	0 ~ 4
B	1	3	2	7	1 ~ 7
C	2	6	4	10	2 ~ 10
D	3	1	-2	5	3 ~ 5
E	4	4	0	8	4 ~ 8
F	5	7	2	11	5 ~ 11
G	6	2	-4	6	6 ~ 6
H	7	5	-2	9	7 ~ 9
I	8	8	0	12	8 ~ 12



Step 2:

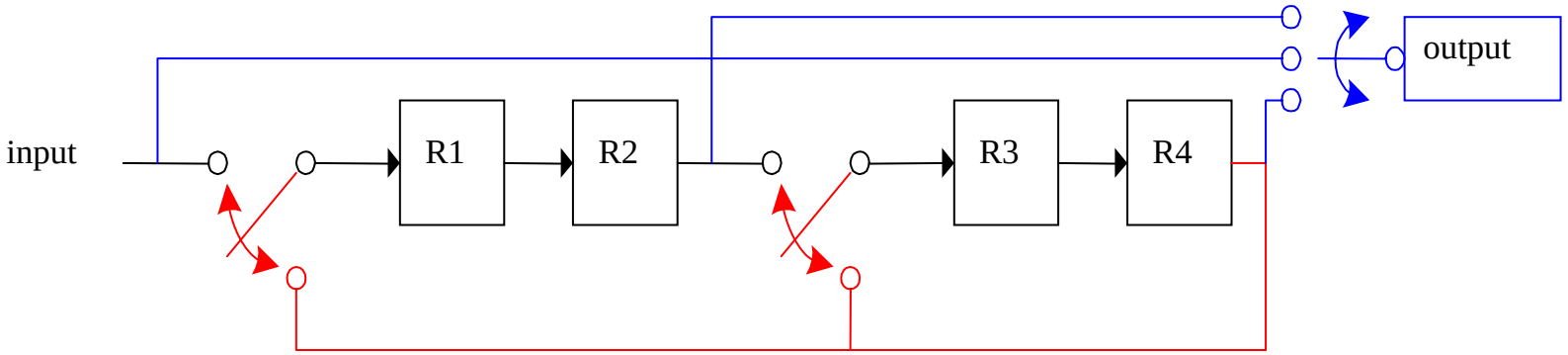
Forward-backward register allocation



cycle	input	R1	R2	R3	R4	output
0	a					
1	b	a				
2	c	b	a			
3	d	c	b	a		
4	e	d	c	b	(a)	a
5	f	e	(d)	c	b	d
6	(g)	f	e		c	g
7	h		f	e		
8	i	h		f	(e)	e
9		i	(h)		f	h
10			i			
11				i		
12					(i)	i

cycle	input	R1	R2	R3	R4	output
0	a					
1	b	a				
2	c	b	a			
3	d	c	b	a		
4	e	d	c	b	(a)	a
5	f	e	(d)	c	b	d
6	(g)	f	e	b	c	g
7	h	c	f	e	(b)	b
8	i	h	c	f	(e)	e
9		i	(h)	c	f	h
10			i	f	(c)	c
11				i	(f)	f
12					(i)	i

Step 3: Hardware Architecture



cycle	input	R1	R2	R3	R4	output
0	a					
1	b	a				
2	c	b	a			
3	d	c	b	a		
4	e	d	c	b	a	a
5	f	e	d	c	b	d
6	g	f	e	b	c	g
7	h	c	f	e	b	b
8	i	h	c	f	e	e
9		i	h	c	f	h
10			i	f	c	c
11				i	f	f
12					i	i

Concluding Remarks

- The same mathematical derivation or algorithm
- Different hardware architecture
  - Area consideration
  - Speed consideration
  - Or, …
- We have to learn more about VLSI signal processing techniques

Course Outline

- Overview
- **Lec 01** : Pipelining & Retiming
  - review of Pipelining & Retiming
- **Lec 02**: Unfolding Transformation
- **Lec 03**: Folding Transformation
  - scheduling
- **Case Study I** : Programmable/Configurable DSP Architectures
- **Lec 05**: Systolic Arrays
- **Lec 06**: Algorithmic Strength Reduction
- **Case Study II**: FFT Processors
- **Lec 08**: Bit-Serial Architectures
- **Lec 09**: Redundant Arithmetic
- **Lec 10**: Numerical Strength Reduction
- **Lec 11**: Distributed Arithmetic

HW for Lec. 0

- 5-by-5 Matrix transposition