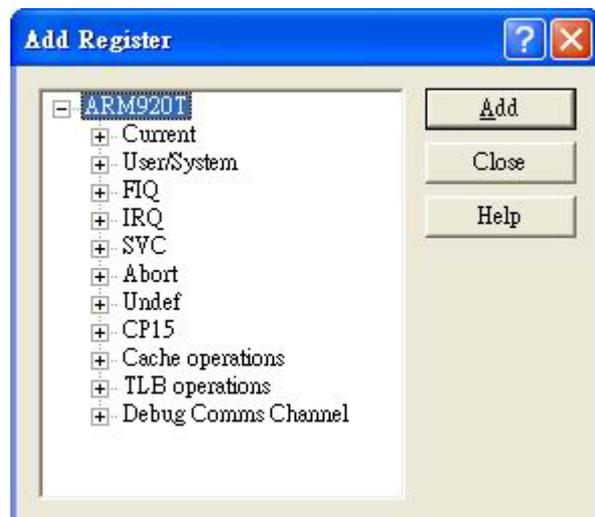


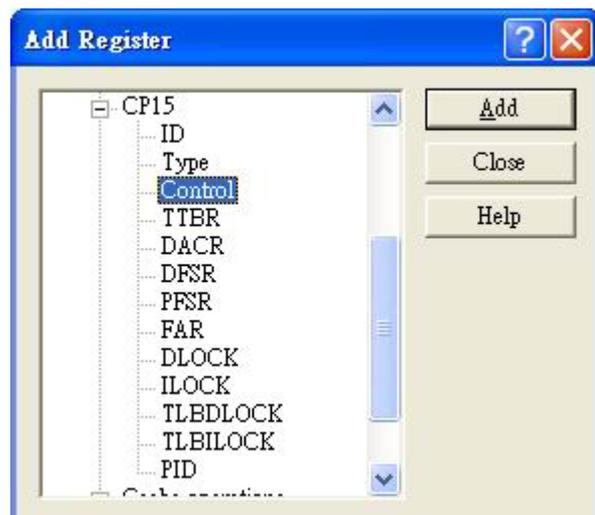
How to disable the cache

Examining the cache status:

1. System View → Registers or press ALT+R, an empty System Registers panel would appear.
2. Right click your mouse and click on Add Registers..., an Add Register window would pop up, click on ARM920T (or the name of the cached core you are using) to show all the system registers.



3. Click CP15 and select Control register and click Add button. Click Close button after finished adding register.



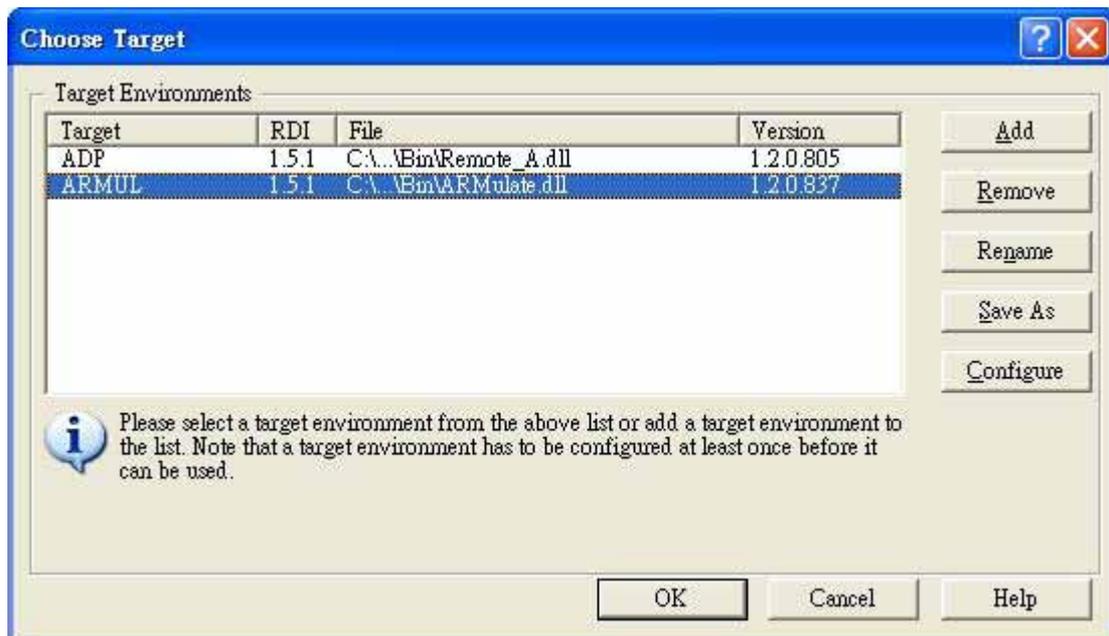
4. The contents of CP15 Control register is shown below. Capital letters mark 1(true, set) and otherwise mark 0(false, cleared). Bit 0 enables MMU when

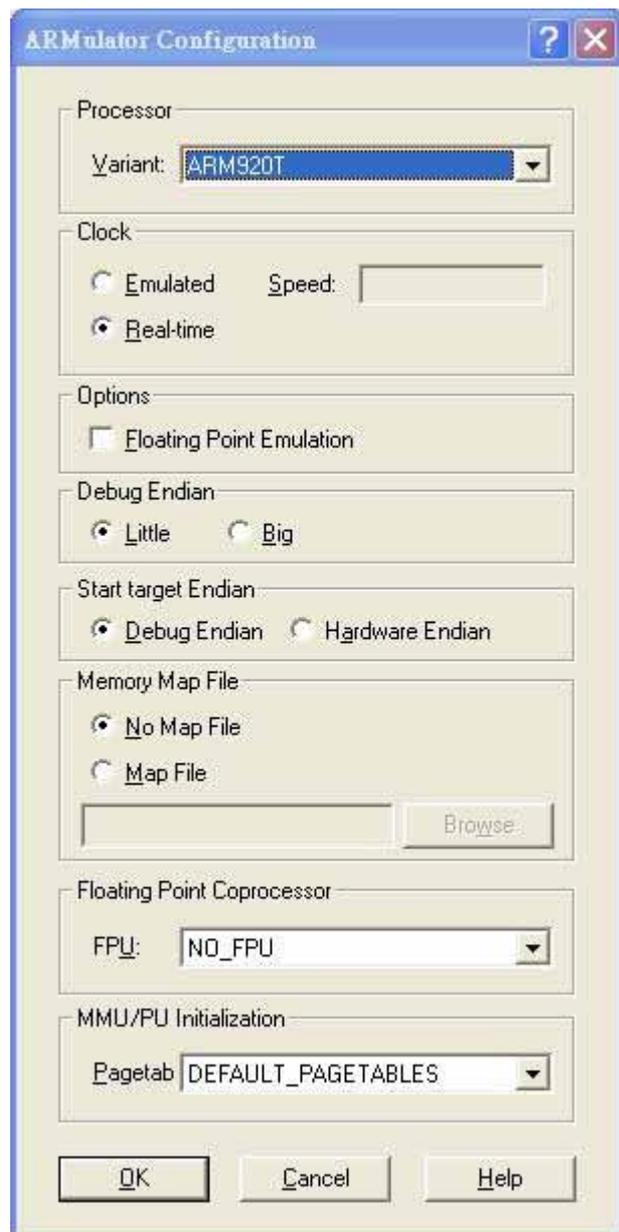
it is set (M), bit 2 enables cache when it is set (C). The cache cannot be enabled unless the MMU is enabled.

Register	Value
ARM920T	{...}
CP15 : Control	Synch_rrvIrshCaM

Disabling cache in ARMulator:

1. Start AXD.
2. Options→Configure Target..., a Choose Target window pops up. Select ARMUL and click Configure button.





3. An ARMulator Configurations pops up, configure the MMU/PU Initialization by setting NO_PAGETABLES shown as follow:



4. Click OK button in ARMulator Configuration window and Choose Target window. AXD would restart using the new configuration.
5. Check cache status using CP15 Control register, the content of Control register should show small letter “c” and “m” for bit 2 and bit 0, this indicates that cache is disabled.

System Registers	
Register	Value
ARM920T	{...}
CP15 : Control	FastBus_rrvirsbcam

Disabling ARM Integrator/Core Module

The cache is disabled as default settings. In order to enable, please refer the core's data sheet and manuals.