SoC Design Laboratory
Term Project Part III
Rapid Prototyping for Baseline JPEG Codec

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In the final part of term project, implement your synthesizable IP with the Logic Module, and prototype the baseline JPEG codec together with ARM Integrator system. Make sure that your codec uses the AMBA-compliant hardware IP you designed in part II.

You have to take the following consideration into account:

- The required HDL files for programming the FPGA on the Logic Module are provided for your reference. Examples for AHB bus interface and structure in Logic Module can be found in ***Install\Logic Modules\LM-XCV600E*** (e.g., C:\Program Files\ARM\Logic Modules\LM-XCV600E\) of PC.

The following documents can be of great help for your project.

- LM-XCV600E User Guide, ***Install\Logic Modules\LM-XCV600E\docs***
- Baselin Motion-JPEG Encoder Description, Amphion, ***http://www.amphion.com/cs6100.html***

Deliverable

Your deliverable has to include:

1. Report that describes your idea and result. Also, your report has to include the following "Sections"
   - Introduction:
     I. As the last part of project, you should summarize the work you have done in the past in this course. Therefore a complete and comprehensive report should be provided by you. This would be taken as a final documentation of your project.
     II. Give a clear and brief description for baseline JPEG codec in the first page.
     III. List the features of your design in a dotted list in the first page. These features should be of real help. The performance of your design is a MUST in the feature list.
   - Architecture:
     I. Describe the system architecture and control scheme related with your IP on the Logic Module.
     II. Draw a block diagram of baseline JPEG codec with your IP. Each block in Logic Module corresponds to the sub-module of your HDL design should be illustrated.
   - Hardware synchronization:
     I. Describe how software synchronizes with your hardware IP.

II. State your considerations and reasons for such synchronization scheme. Also discuss the consequences of the synchronization scheme.

- Memory Requirements:
  I. List the memory map and the usage of your system.
  II. Compare the memory needs of the system without hardware IP and the hardware accelerated one.
- Performance:
  I. Show your performance. Compare it with the system without hardware IP. You can use the *time (null)* function if it is needed.
  II. Discuss on the performance result you obtain. If it's improved, state the reason. If it's not improved, state why it failed.
- Verification:
  I. How you verify the functionalities.
  II. Verification results
- File Lists:
  I. Description of each file in your project.

2. Source code of your IP, driver program, application software codes.
3. All setting and information required for regenerating the result shown in your report. If the results of your design cannot be regenerated by using your information, the report will not be recognized.
4. Please acknowledge in the last section of your report that you've used the reference code and related documents.

State your approaches, key ideas and results clearly and formally, and avoid redundant description. Your report can be written in Chinese or English. However, make sure your report is readable. A manual report won't degrade your score, unless it is scrabbled.

For more information

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