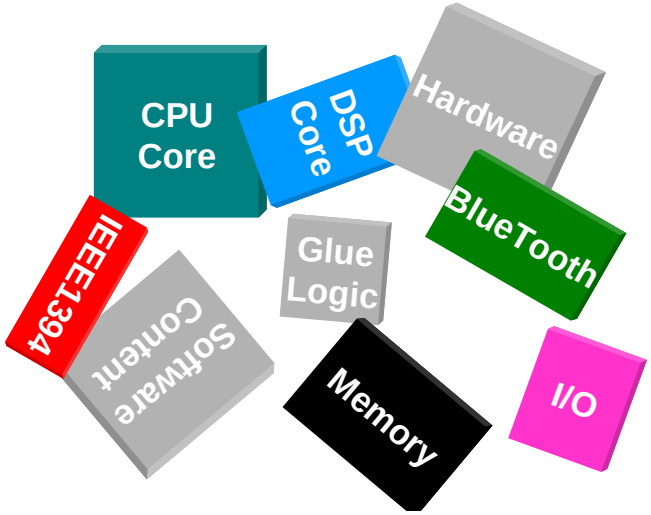
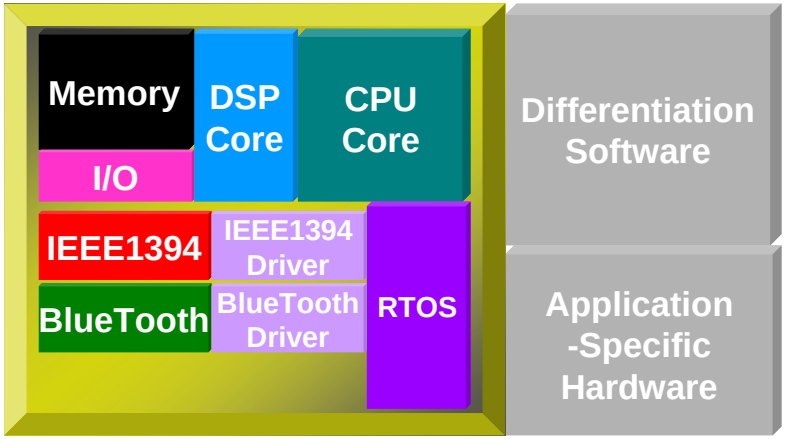
Platform-based Design

The New System Design Paradigm



Block-Based Design



Platform-Based Design

Orthogonalization of concerns: the separation of function and architecture, of communication and computation

Terms

- Function
  - A function is an abstract view of the behavior of the system.
  - It is the input/output characterization of the system with respect to its environment.
  - It has not notion of implementation associated to it.
- Architecture
  - An architecture is a set of components, either abstract or with a physical dimension, that is used to implement a function.
- Architecture platform
  - A fixed set of components with some degrees if variability in the performance or dimensions of one or more of its components

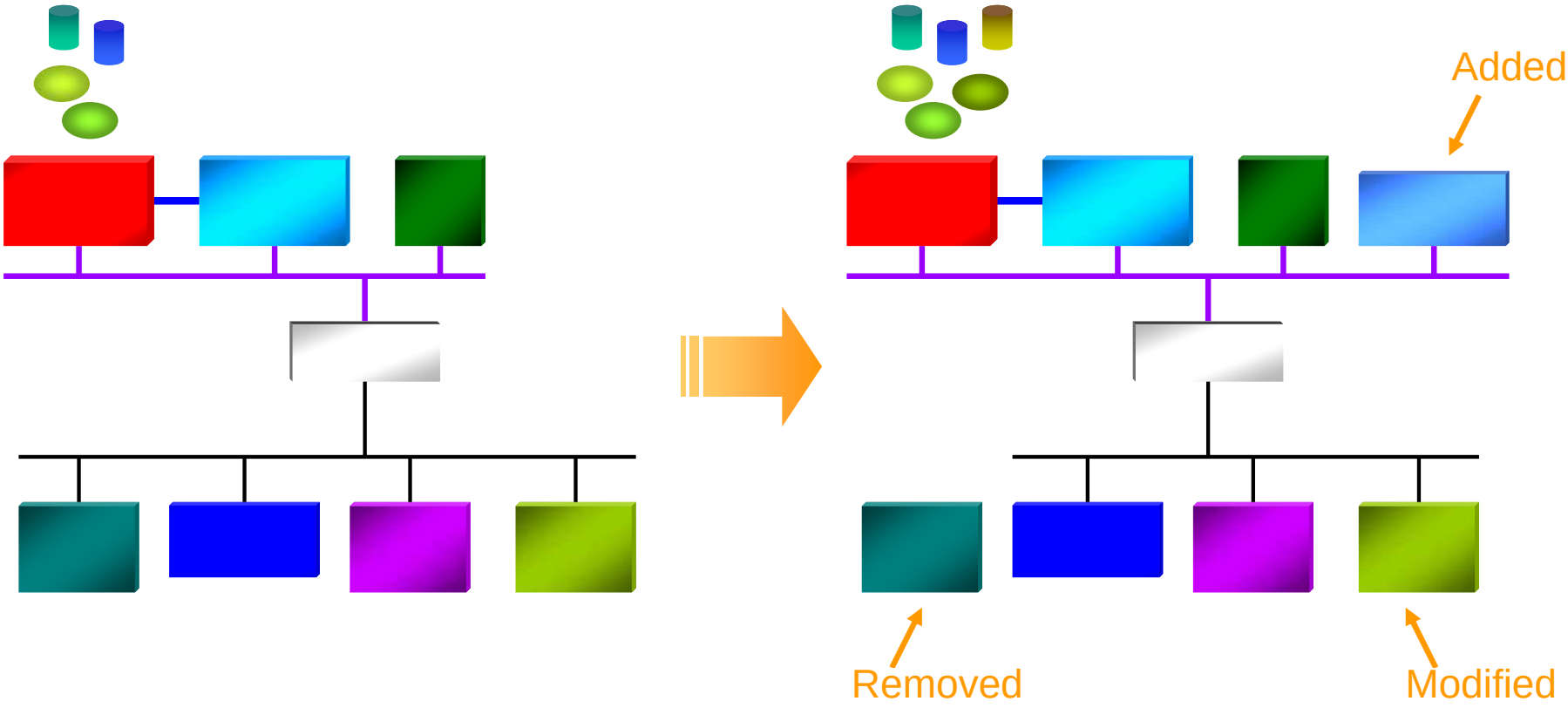
Communication

- Communication provides for the transmission of data and control information between functions and with the outside world.
- Communication layers
  - Transaction: Point-to-point transfers between VCs. Covers the range of possible options and responses (VC interface).
  - Bus Transfer: Protocols used to successfully transfer data between two components across a bus.
  - Physical: Deal with the physical wiring of the buses, drive, and timing specific to process technology.

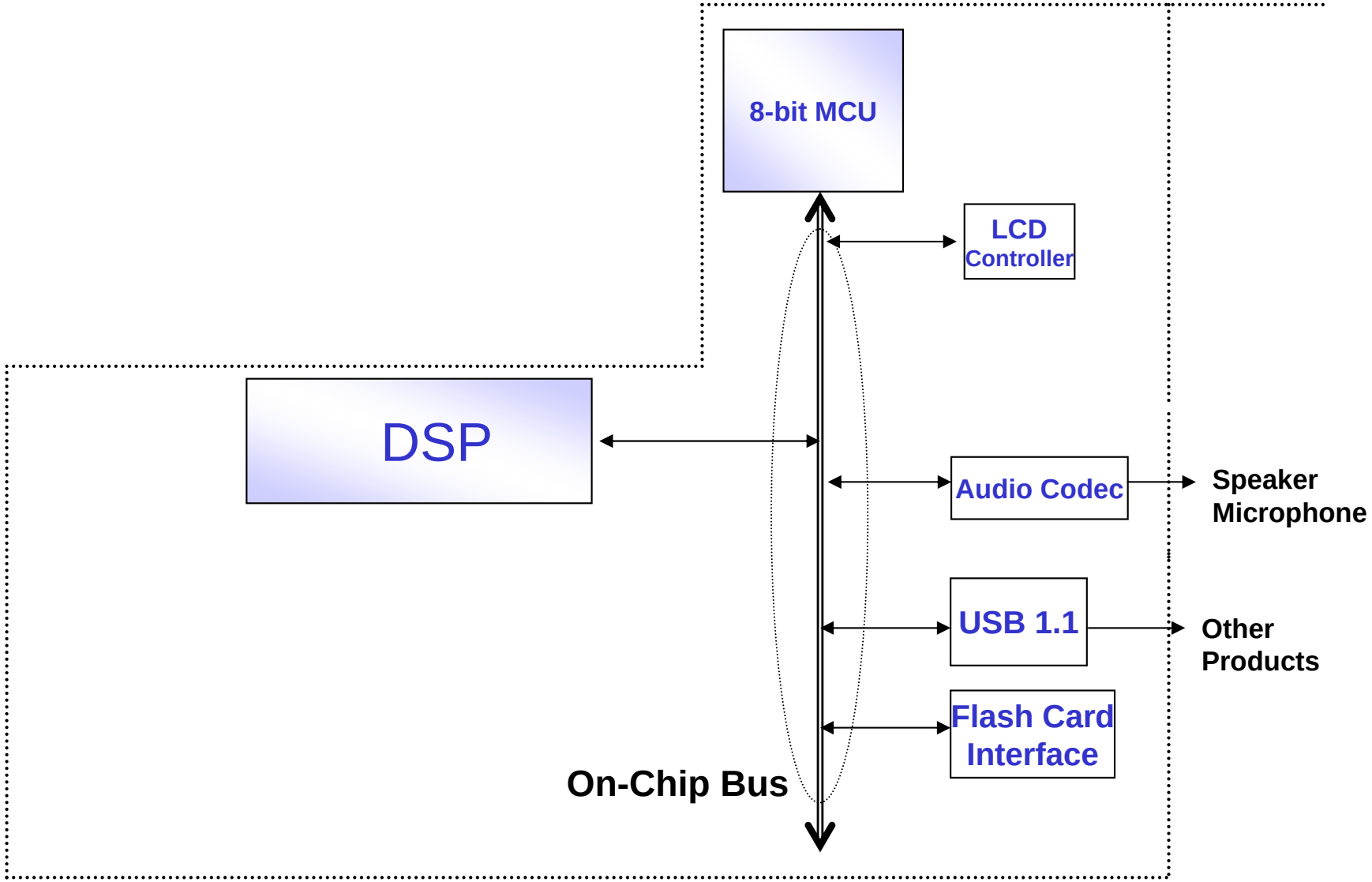
How Platform-Based Design Works?

Reference design

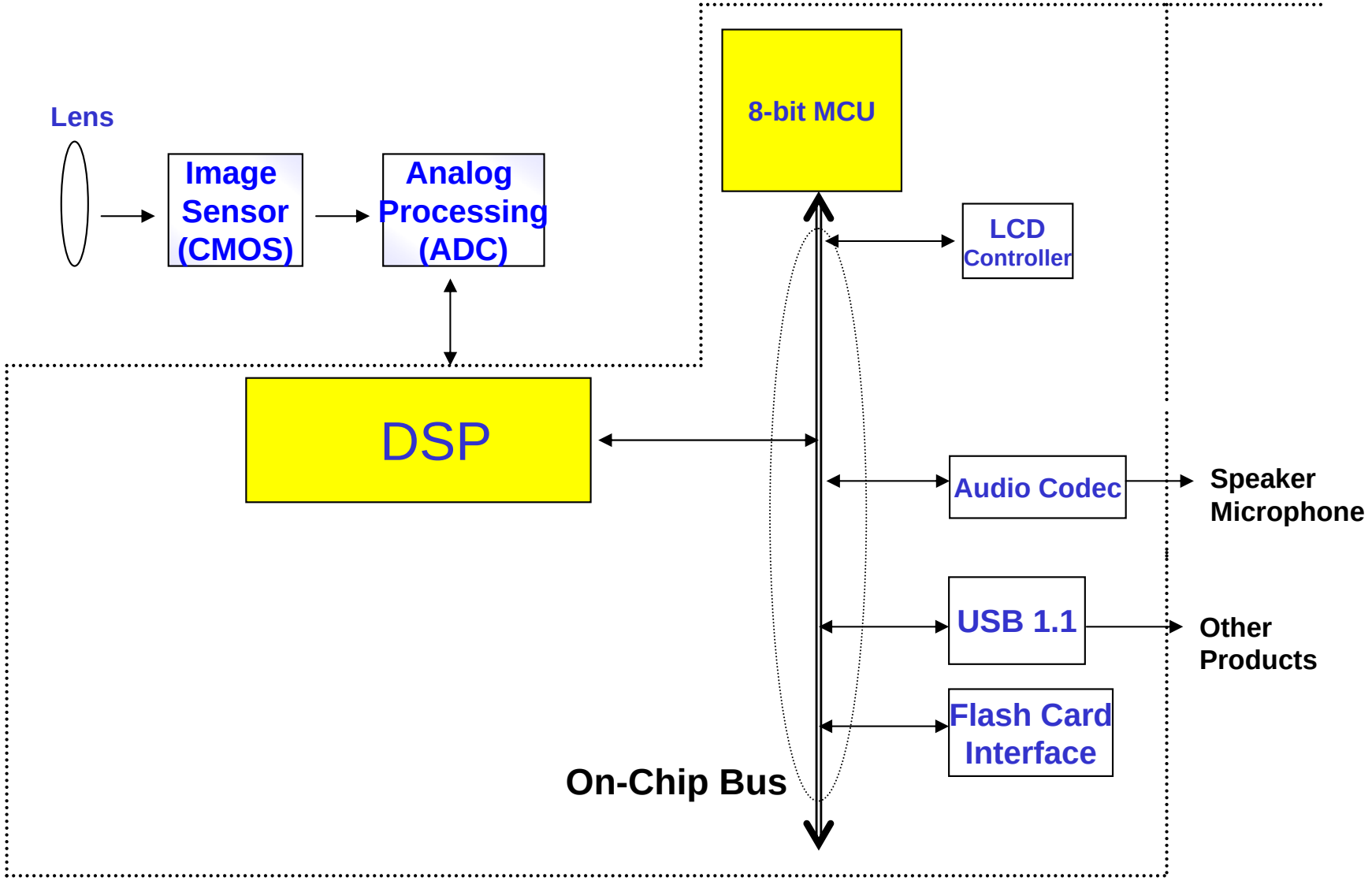
Derivative design



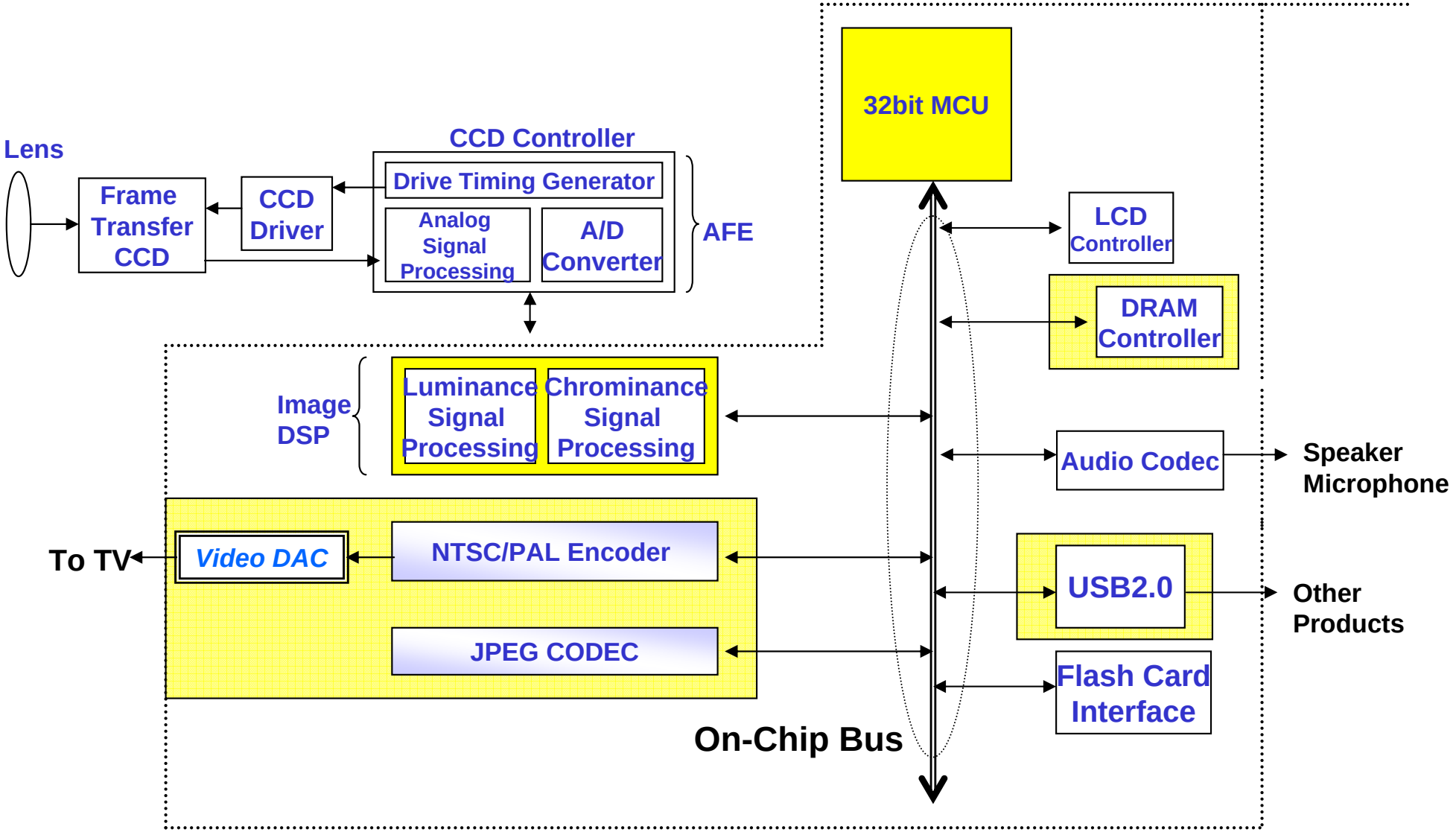
Multimedia Platform: MP3



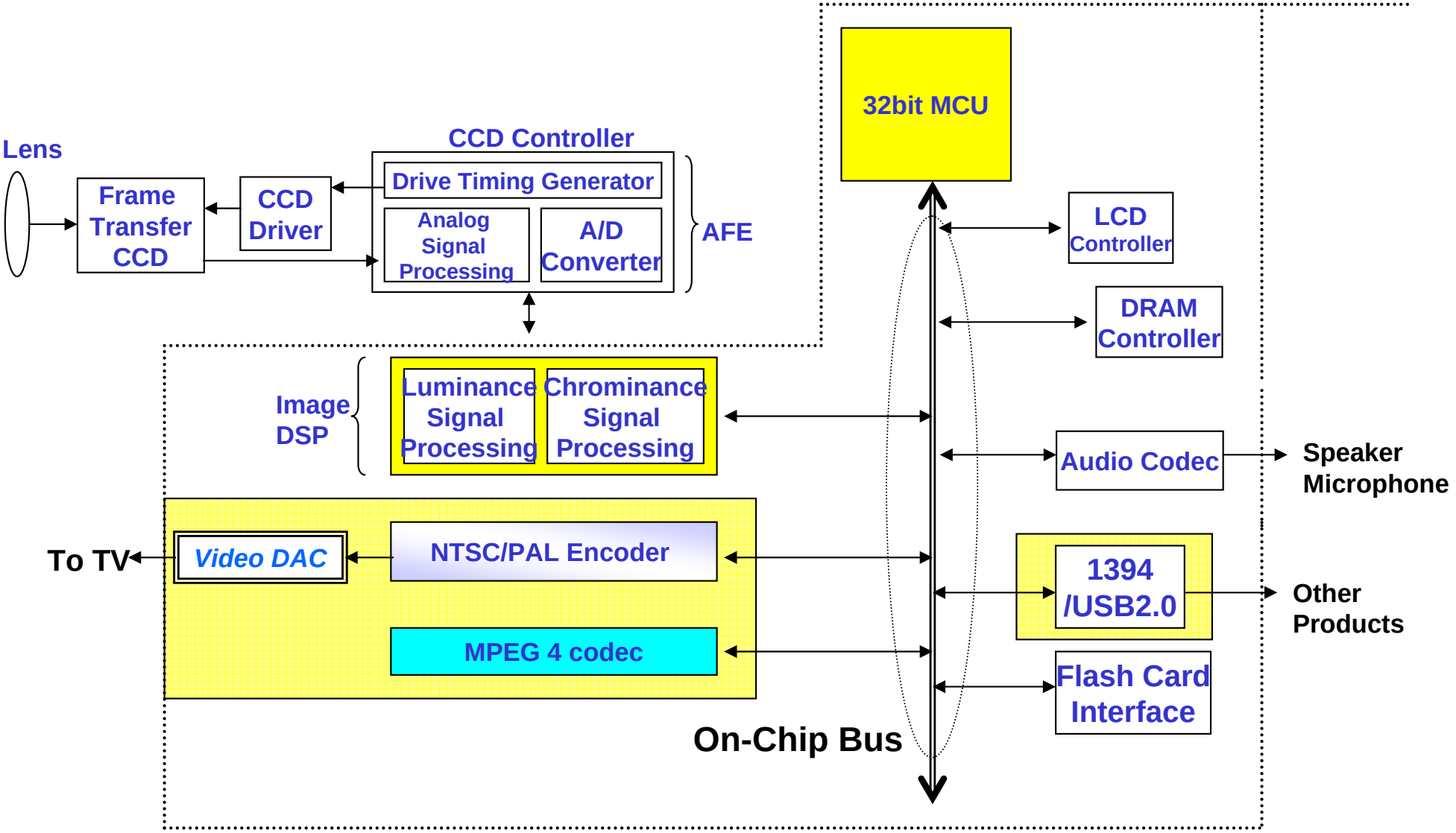
Multimedia Platform: PC Camera



Multimedia Platform:DSC



Multimedia Platform: Video Camera

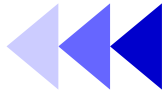


Platform-based integration

- A fully defined architecture with
  - Bus structure
  - Clocking/power distribution
  - OS
- A collection of IP blocks
- Architecture reuse

The definition of a hardware platform is the result of a trade-off process involving reusability, production cost and performance optimization.

Ingredients of A Platform



- Cores
  - Processor IP
  - Bus/Interconnection
  - Peripheral IP
  - Application specific IP
- Software
  - Drivers
  - Firmware
  - (Real-time) OS
  - Application software/libraries
- Validation
  - HW/SW Co-Verification
  - Compliance test suites
- Prototyping
  - HW emulation
  - FPGA based prototyping
  - Platform prototypes (i.e. dedicated prototyping devices)
  - SW prototyping

How to Build A Platform

- Architecture constraints for an integration platform:
  - first pick your application domain
  - then pick your on-chip communications architecture and structure (levels and structure of buses/private communications)
  - then pick your Star IP (e.g. processors) – processors 'drag' along detailed communications choices e.g. processor buses,
  - dedicated memory access, etc. - ARM-AMBA, etc. Also limit e.g. RTOS
  - pick application specific HW and SW IP
  - other IP blocks not available 'wrapped' to the on-chip communications may work with IP wrappers. VSI Alliance VCI is the best choice to start with for an adaptation layer

Pros & Cons of Platform-based Design Design

- Advantages
  - Can substantially shorten design cycles
  - Large share of pre-verified components helps address the validation bottleneck for complex designs
  - Enables quick derivative designs once the basic platform works
  - Rapid prototyping systems can be used to quickly build physical prototypes and start S/W development
- Limitations
  - Limited creativity due to predefined platform components and assembly
  - Differentiation more difficult to achieve, needs to be primarily in application software

Platform-summary

- What is a platform - a shortcut to time-to-market
  - Object
    - Architecture reuse
    - HW/SW co-design
  - Accessory: tools, design and test methodologies
- How to differentiate a platform
  - Programmability, Configurability, Scalability, Robustness
  - Performance, Area, Power
  - Application softwares
- Intention
  - Prototyping, product

Types of Platform

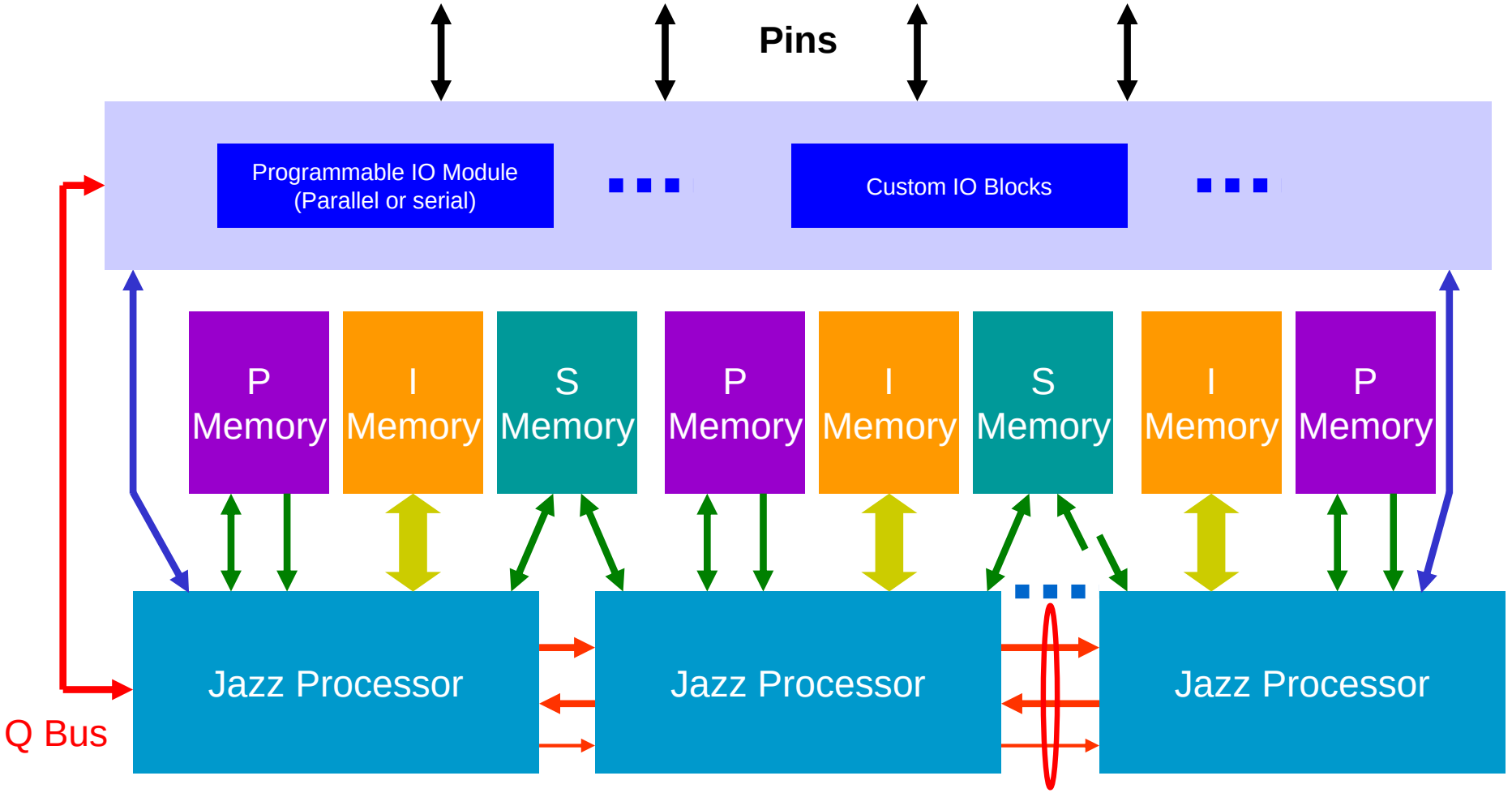
- According to the strength of constraints on hardware

stronger

  - Fixed Platforms
    - Software-oriented: TI's OMAP™, Philips Nexperia™.
    - Application-specific: Ericsson's BCP,
  - Configurable platforms
    - Bus structure, multiple processor, programmable logic device
    - E.g.: Altera's Excalibur™, Triscend's CSoC, Philips RSP, Cypress MicroSystems' PSoC™, E.g.: Palmchip's PalmPak™, Wipro's SOC-RaPtor™ , Tality's ARM-based SoC.
  - Programmable platform
    - Improv's - PSA™ Jazz

weaker

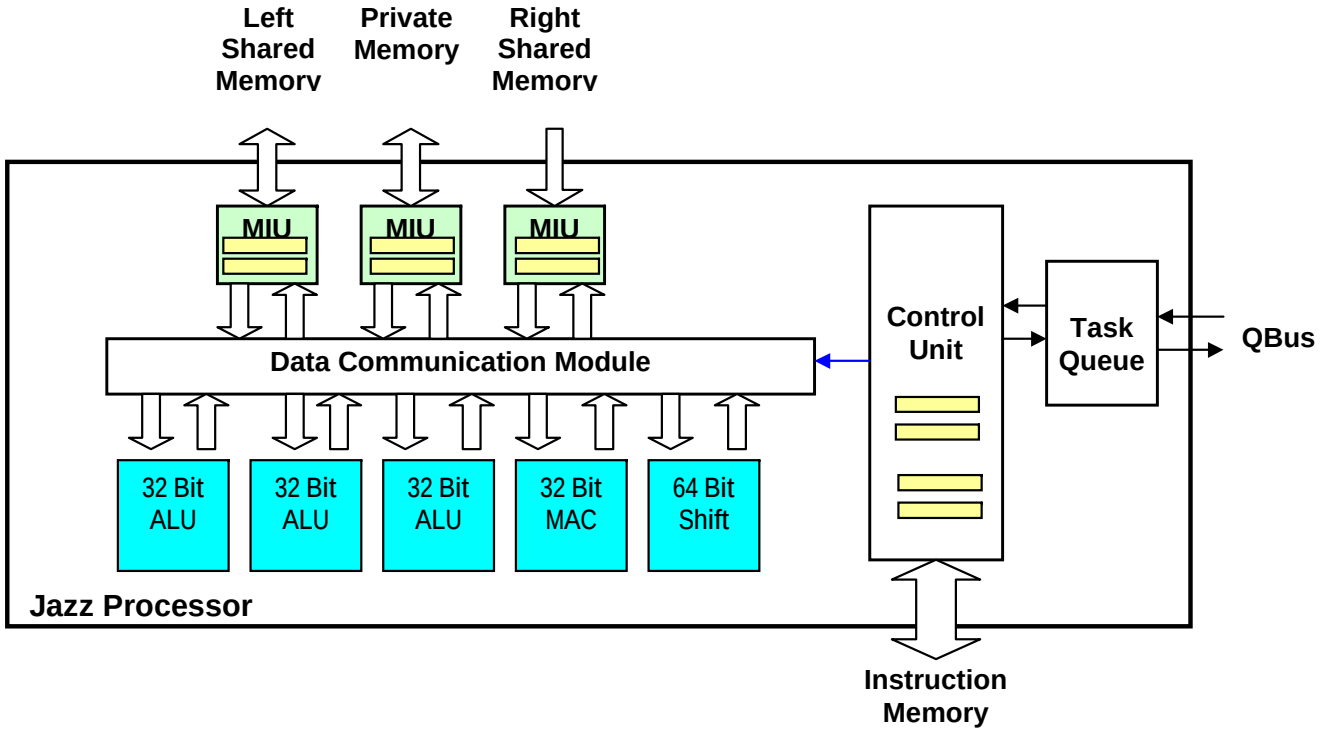
Improv - PSA™ Jazz Platform



Acronym
- I : Instruction
- P: Private:
- S: Shared

Q Bus (Queue Bus)
- QBus-A
- Qbus-B
- Arb

Jazz VLIW Processor - A Sample

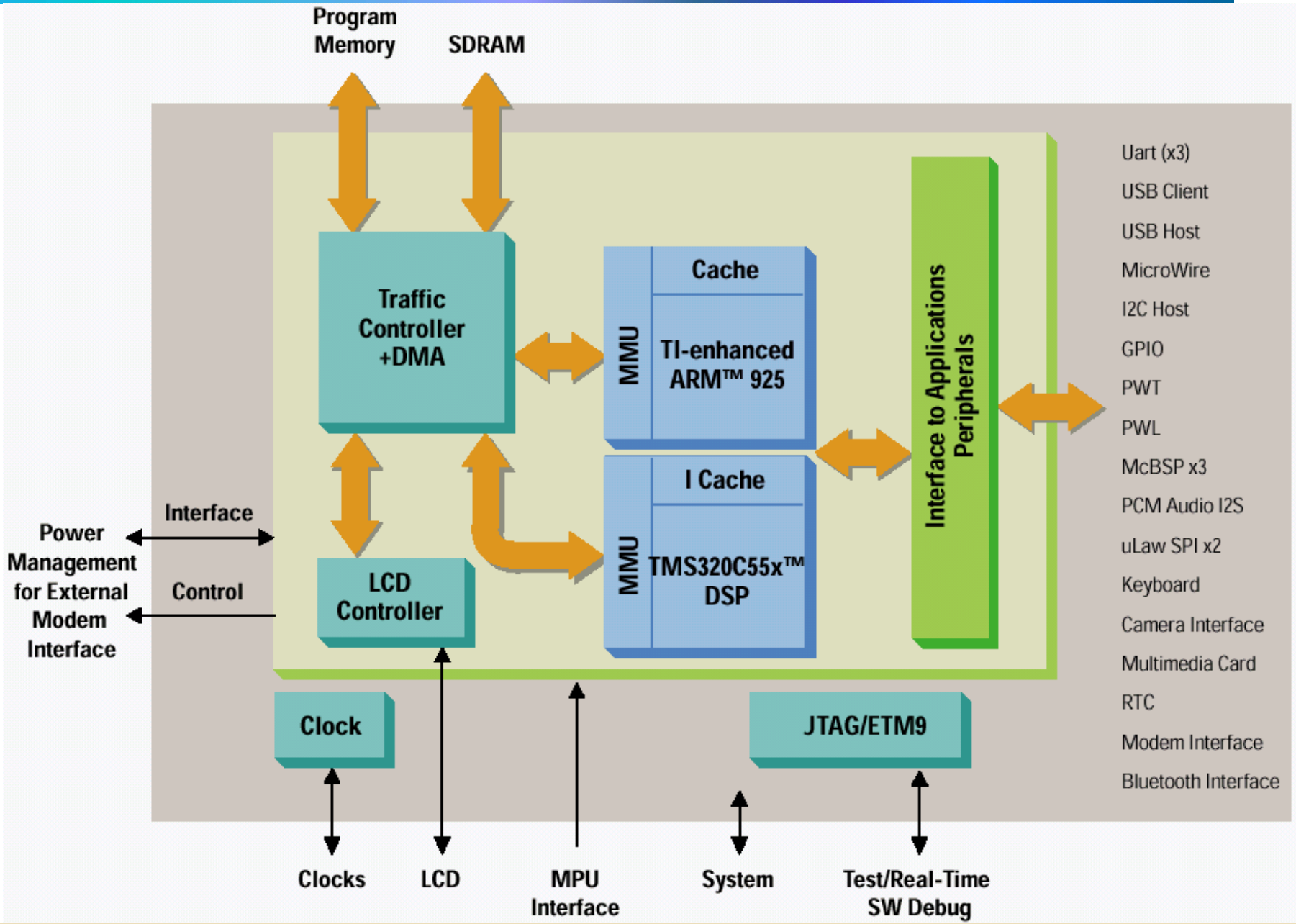


- 3 ALUs, 1 MAC, 1 SHIFT, 1CNT (built into control unit)
- 240 bit instruction width (memory image lower using instruction compression)
- 32-bit datapath, 16-bit address width
- 32 deep Task Queue
- 1.3 BOPS at 100 MHz (5 CU ops, counter, 7 MIU ops)
- ~100K gates

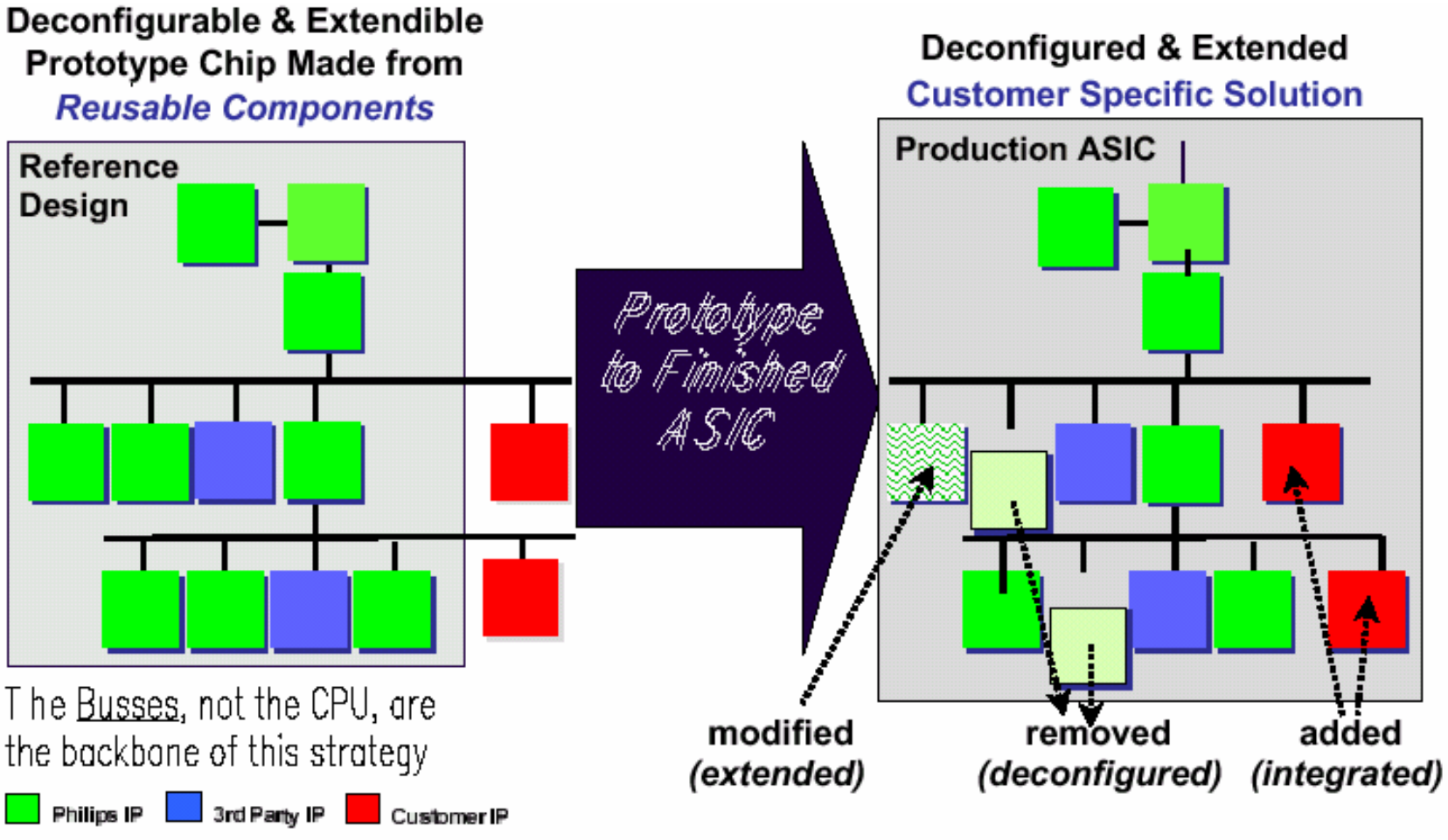
Features

- State-of-the-art compilation technology that supports both
  - Task level parallelism (with the multiple processors)
  - Instruction level parallelism (through the Jazz VLIW processors).
- Designer start at the Java level
- No OS required
- Configuration at three levels
  - Platform - Collection of processors, data/instruction memory and I/O resource
  - Processor - Computation units and memory interfaces
  - Instruction - User can create custom logic computation units

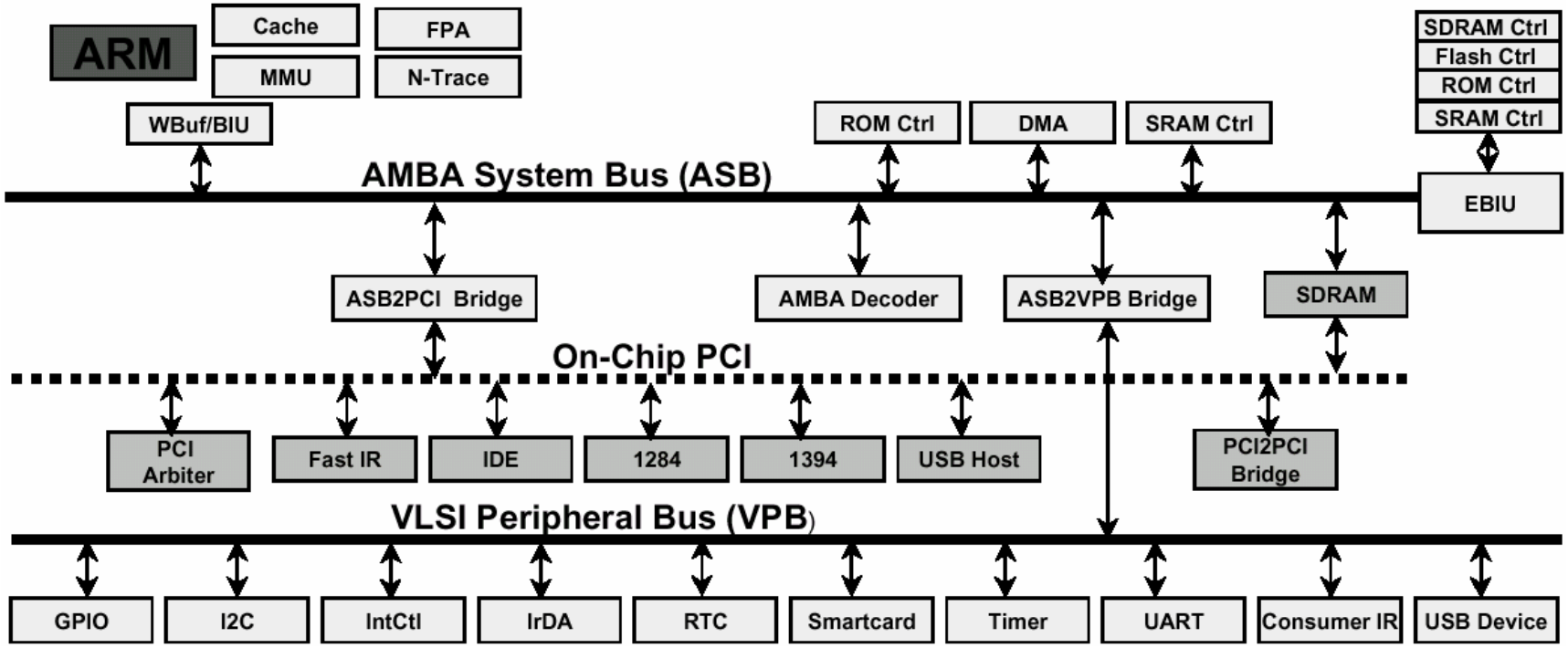
TI's OMAP™ Platform



Philips - Rapid Silicon Prototyping (RSP)



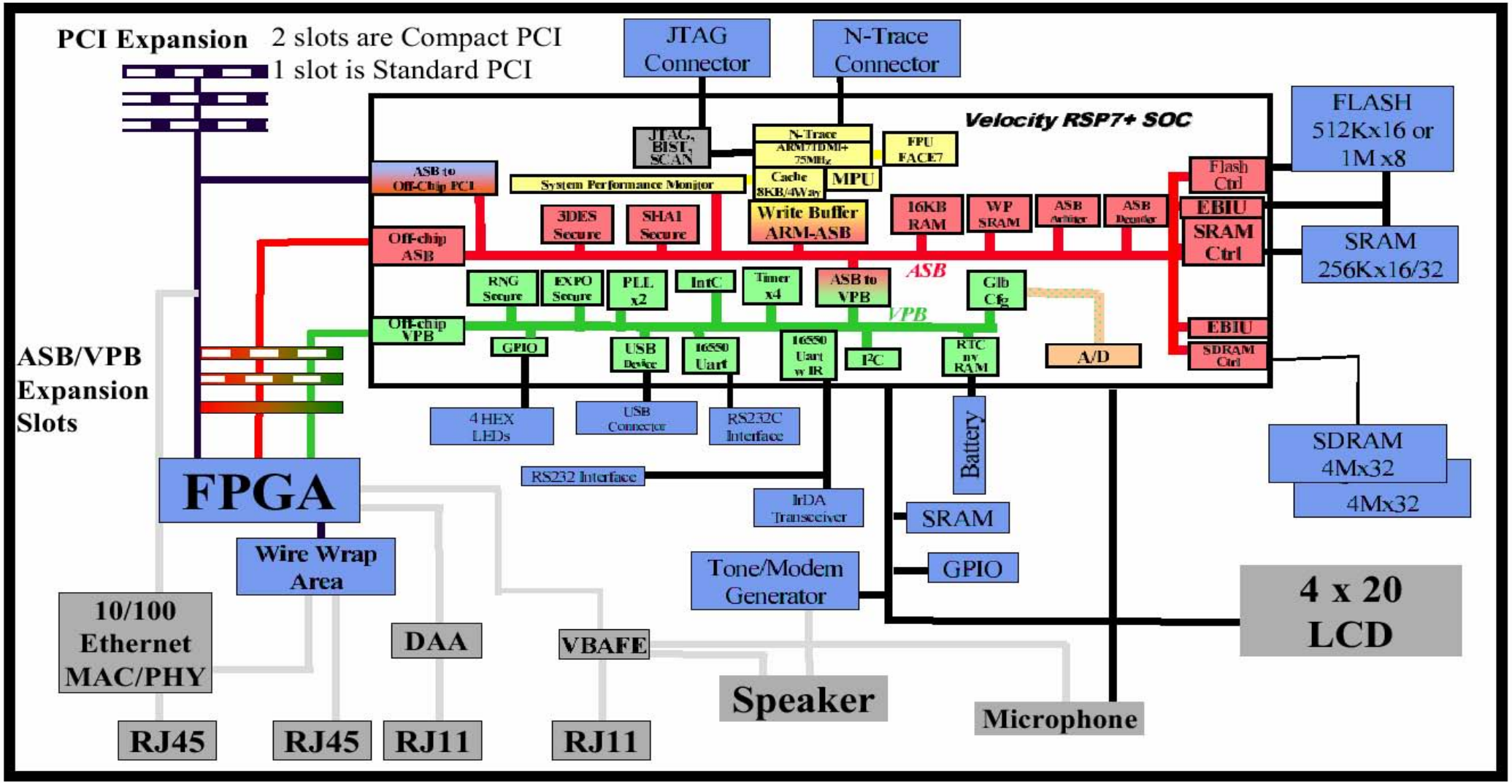
RSP7 ASIC Block Diagram



RSP7+ is targeted at customer designing SOC ASICs for:

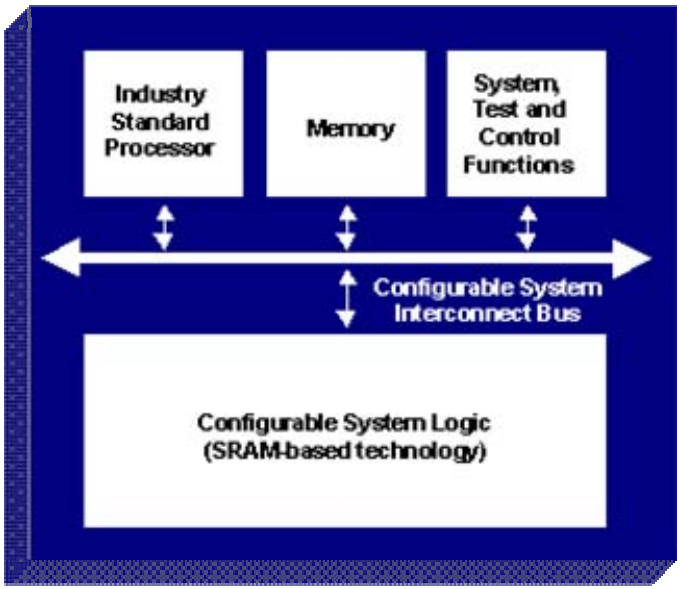
- **Networking Peripherals**
- **Virtual Private Networks**
- **Systems Requiring ARM-based Control and Wired Connectivity**

RSP7+ Emulation Board

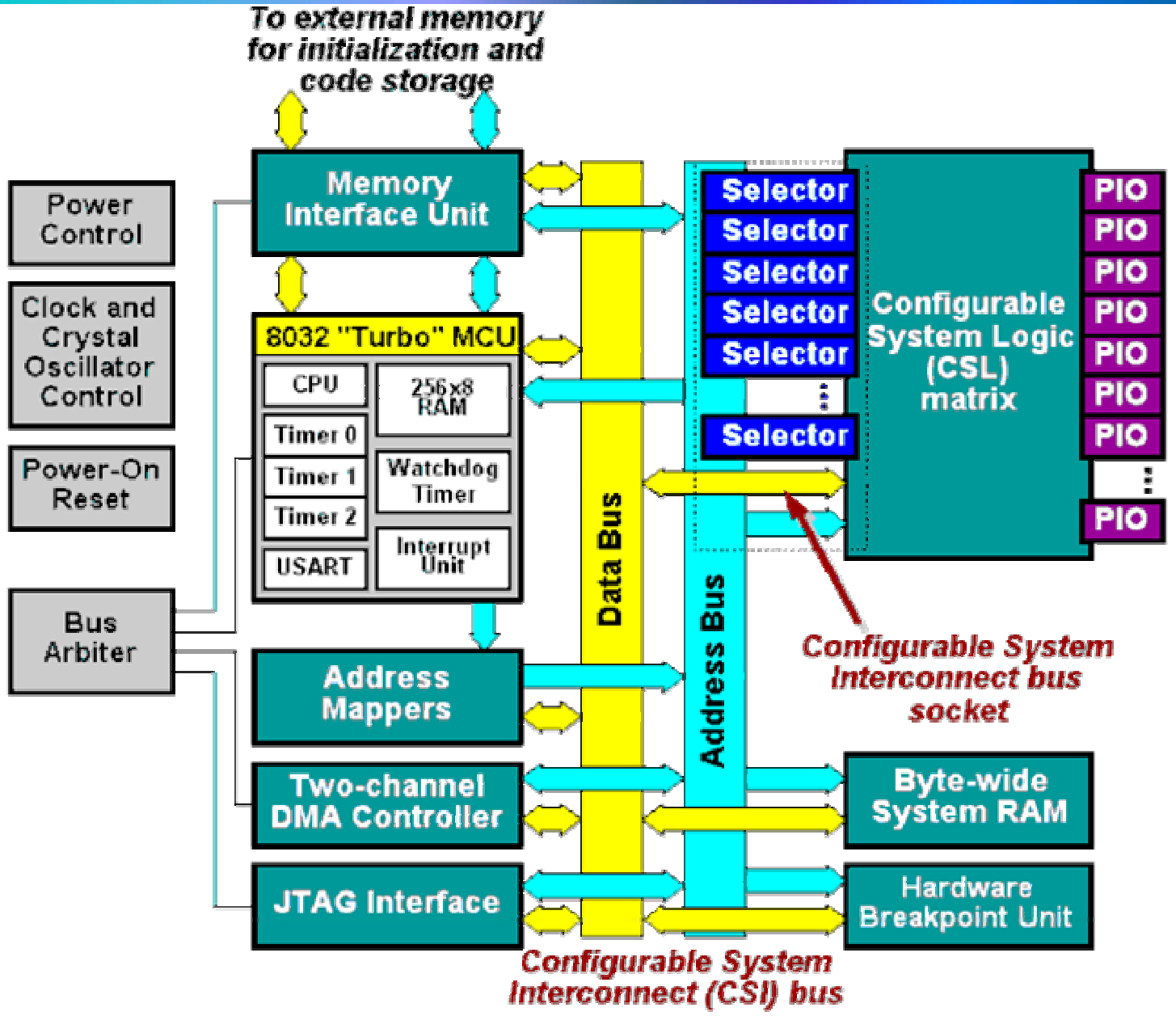


Triscend - Configurable System-on-Chip

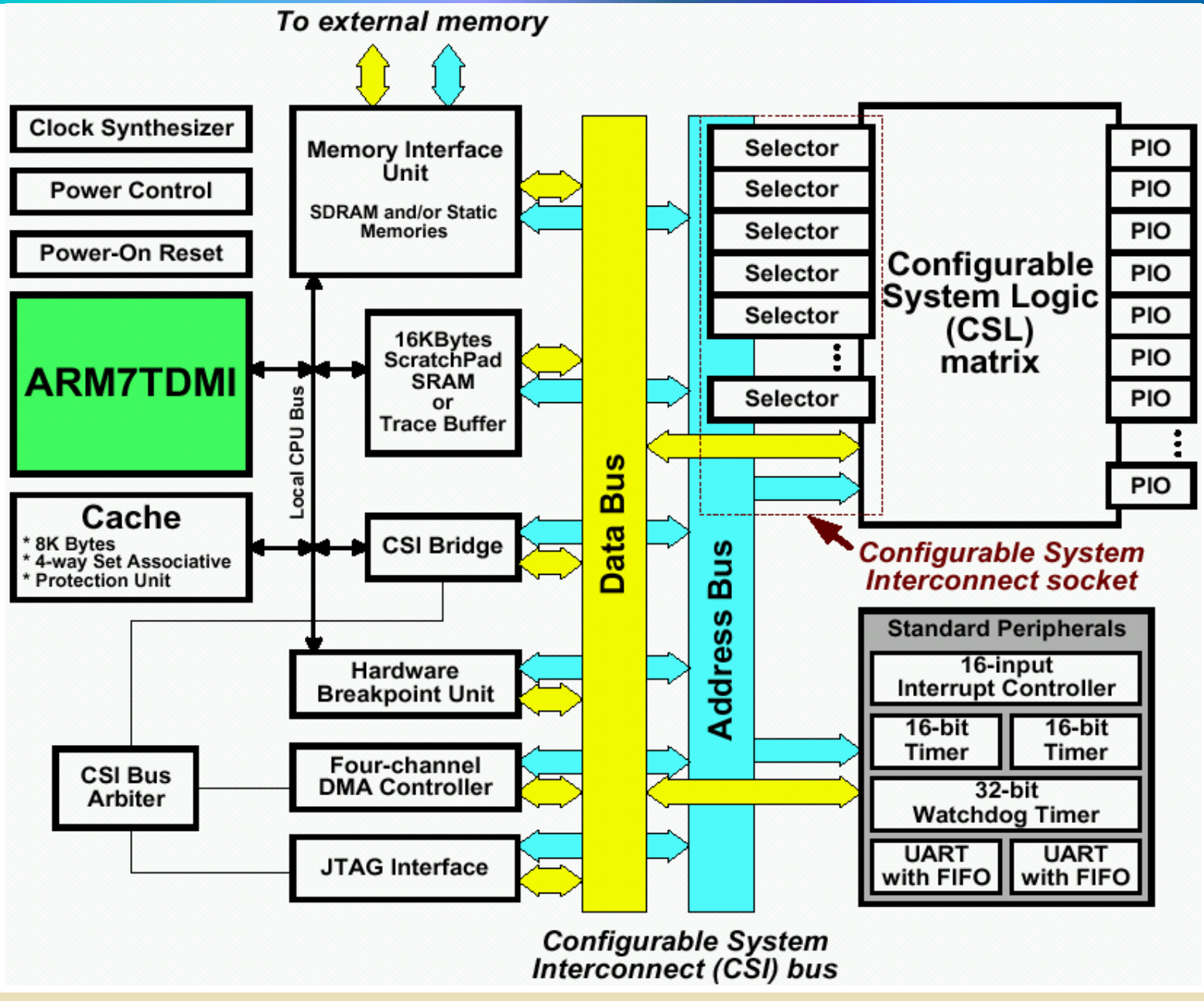
- A configurable system-on-chip (CSoC) is a single device consisting of:
  - A dedicated, industry-standard processor
    - 8051-based E5a
    - ARM-based for A7 device
    - SuperH for the future (2001.1.22 announced, 2002 available)
  - An open-standard, dedicated, on-chip bus
  - Configurable logic
  - Memory
  - Other system logic



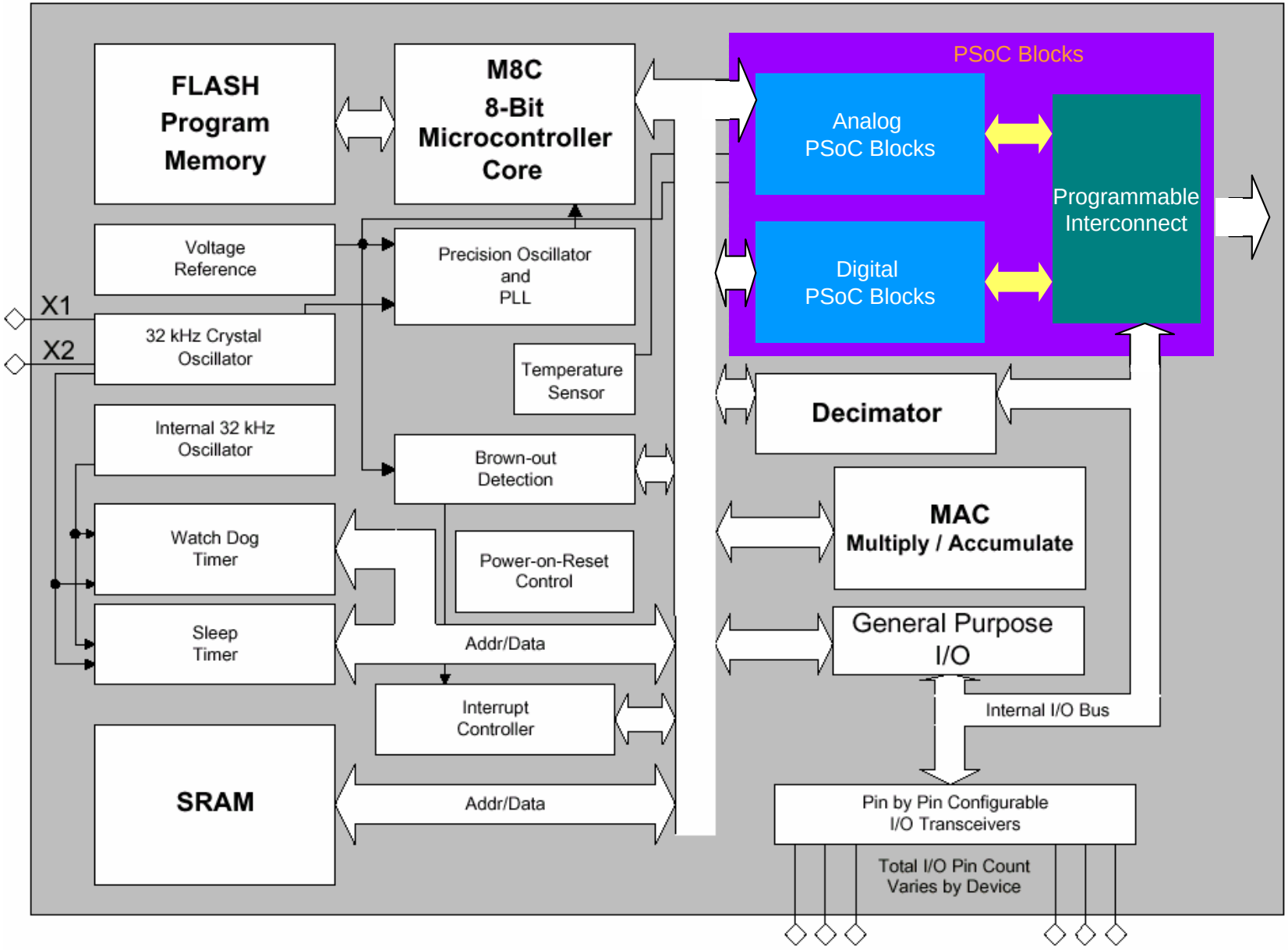
Triscend E5 System Highlights



Triscend A7 System Highlights



Cypress MicroSystems - PSoC™

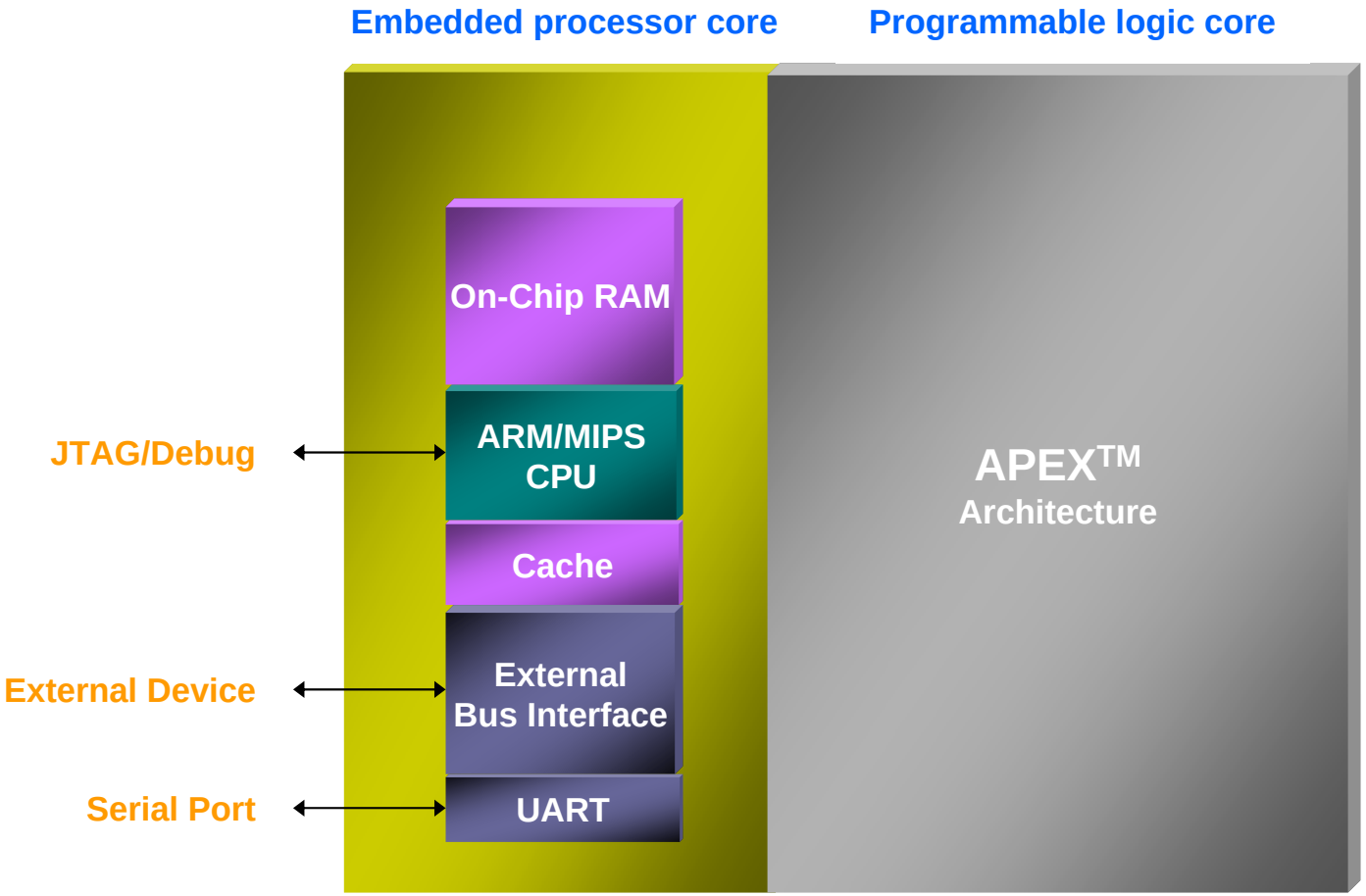


PSoC Blocks

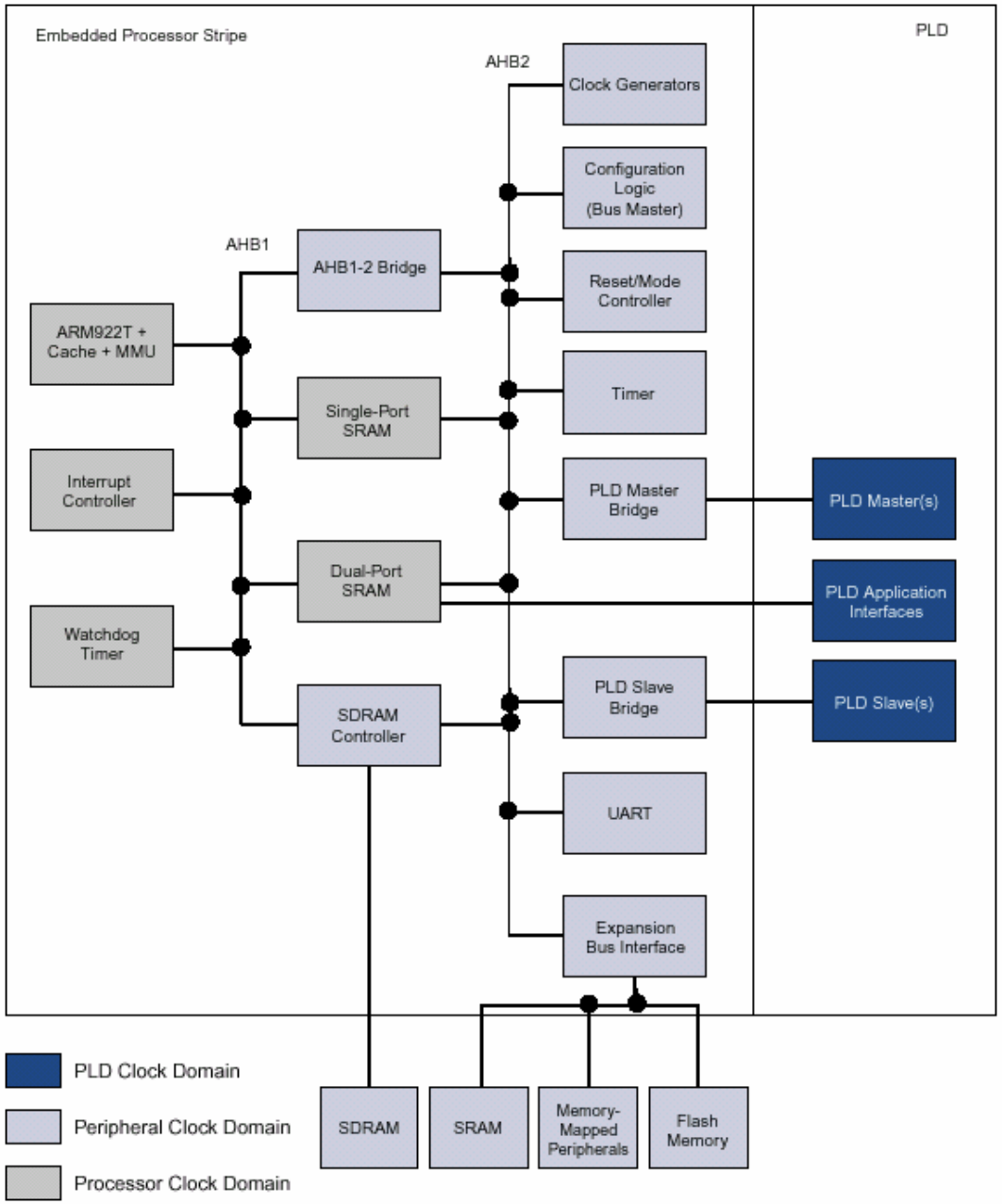
- Eight 8-bit digital PSoC blocks
  - Four Digital Basic Type A blocks:
    - Timer/Counter/Shifter/CRC/PRS/Deadband functions
  - Four Digital Communications Type A blocks:
    - Timer/Counter/Shifter/CRC/PRS/Deadband functions
    - Full-duplex UARTs and SPI master or slave functions
- Twelve analog PSoC blocks
  - Three types: ContinuousTime (CT) blocks, and type 1 and type 2 Switch Capacitor (SC) blocks that support
  - 14 bit Multi-Slope and 12 bit Delta-Sigma ADC, successive approximation ADCs up to 9 bits, DACs up to 9 bits, programmable gain stages, sample and hold circuits, programmable filters, differential comparators, and temperature sensor.

Altera - Excalibur™ Embedded Processors

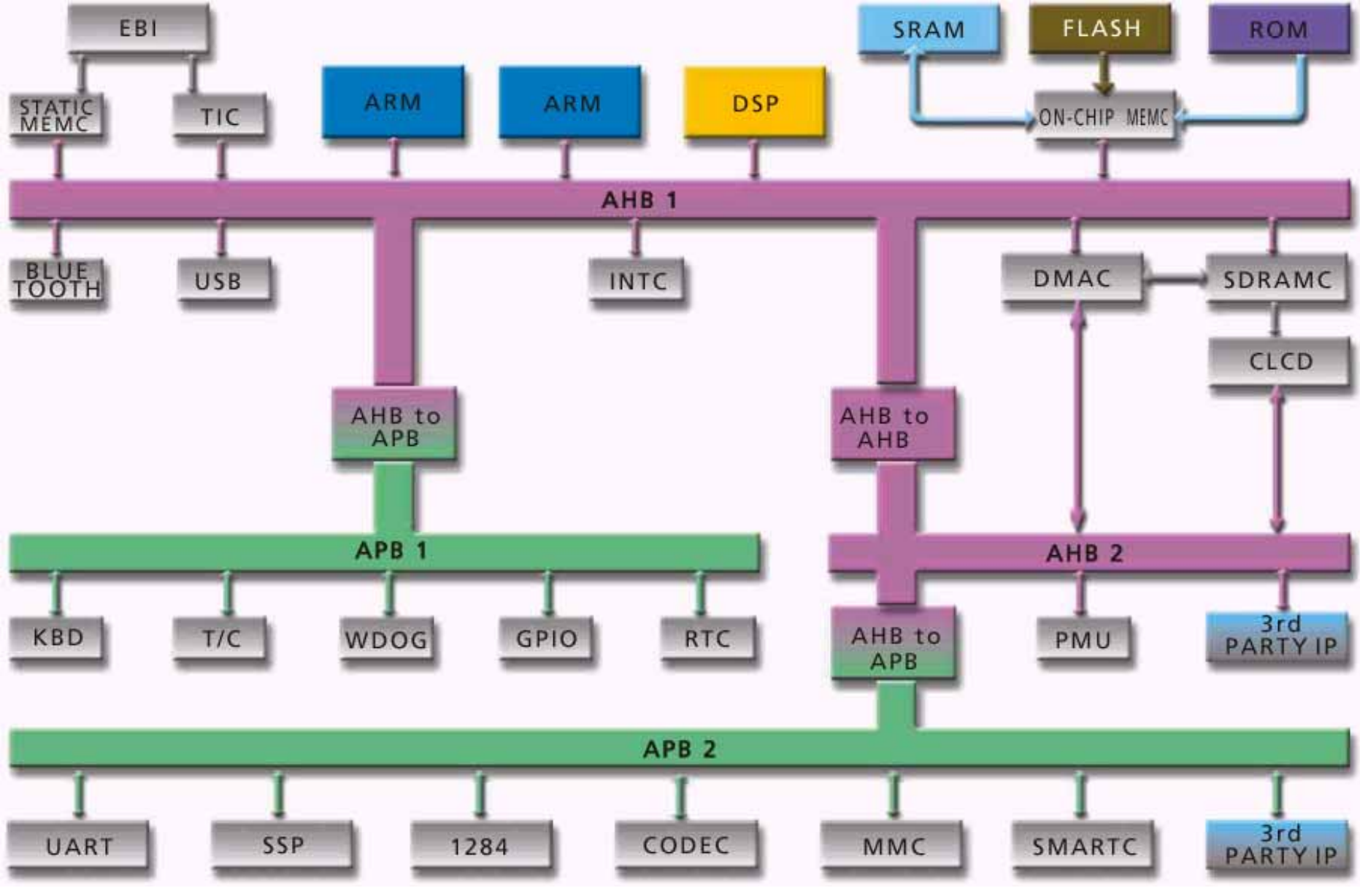
- Processors
  - ARM, MIPS



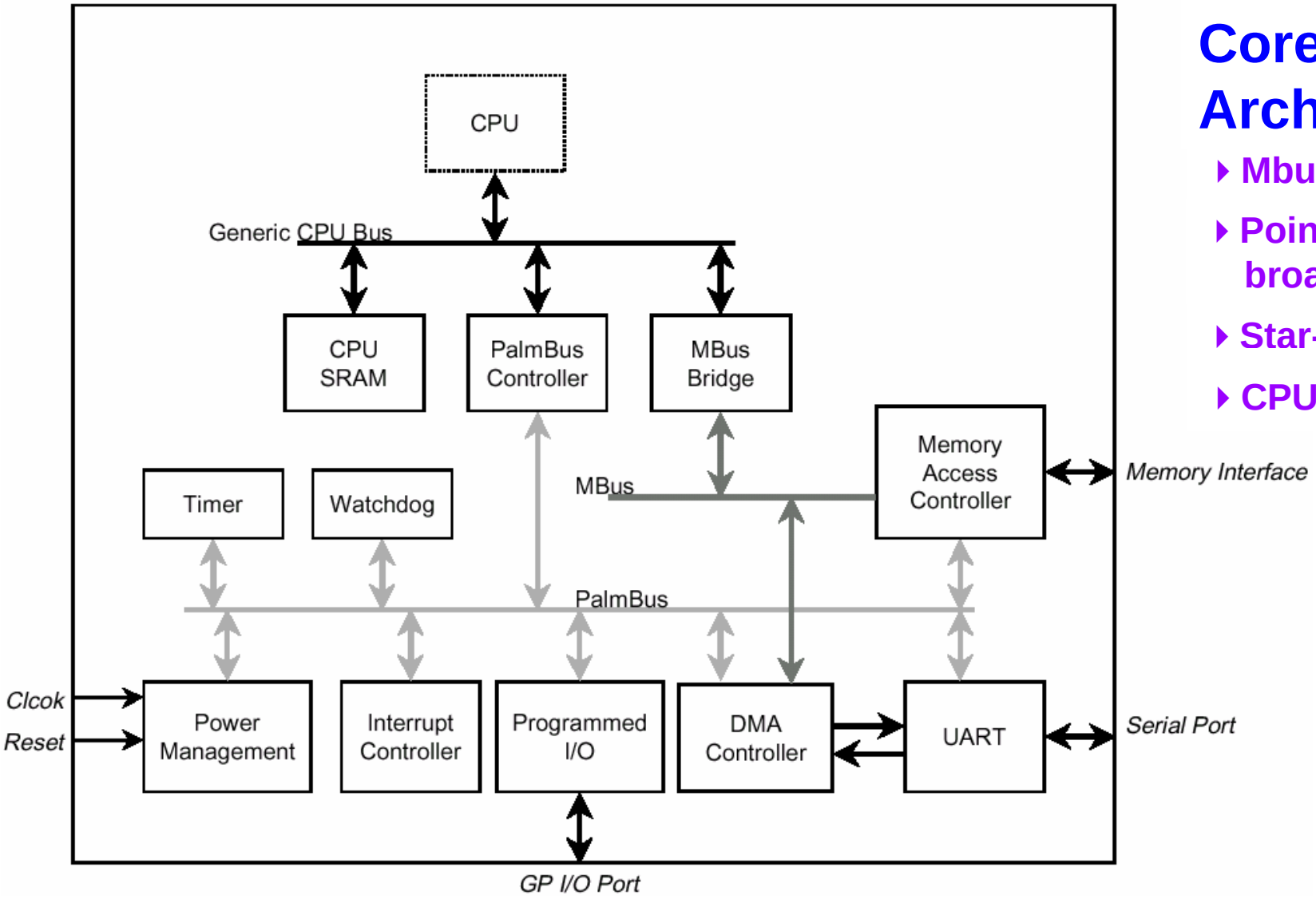
ARM-Based System Architecture



Wipro's SOC-RaPtor™ Architecture



Palmchip's PalmPak™ SoC Platform

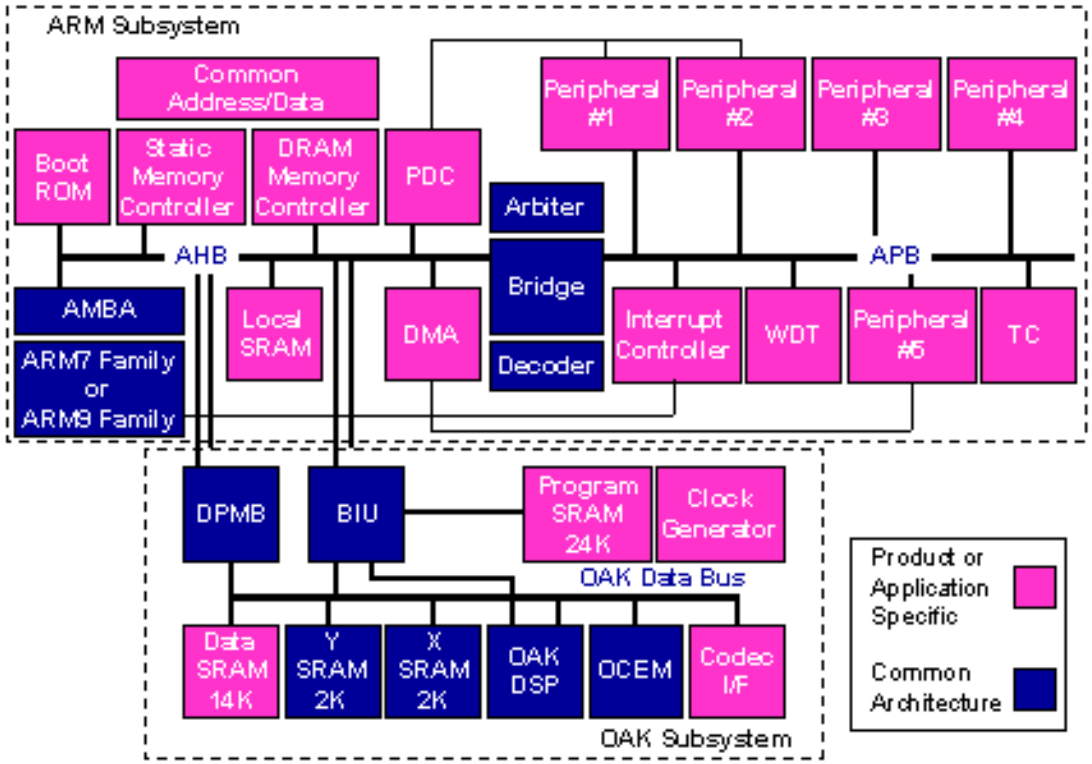


CoreFrame™ Architecture

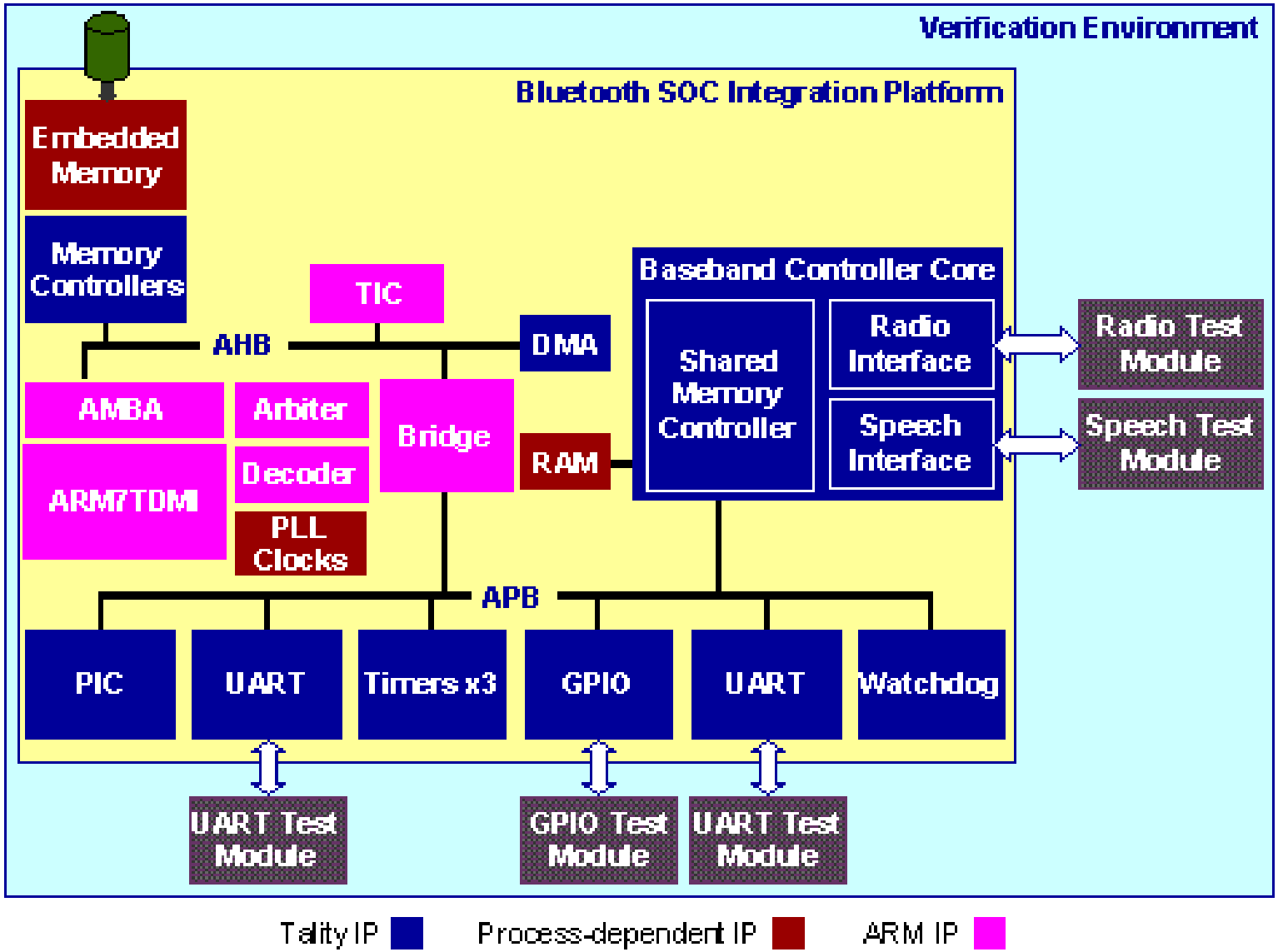
- Mbus and PalmBus
- Point-to-point and broadcast connections
- Star-shaped topology
- CPU Subsystem

Tality's ARM/OAK-based SoC Platform

- Used as the development vehicle for multiple application-specific Integration Platforms.
  - for Bluetooth, xDSL and Cable Modems.
  - "Socketizes" the IP to make it AMBA 2.0-compliant.



Example of Tality's Derived Design - Bluetooth



Summary

- Platform-based design
  - From board design to SoC design
  - From executable spec., i.e., C/C++, to SystemC
- Modeling
  - Performance evaluation
  - Task mapping
  - Communication refinement