On-Chip Bus Overview

Outline

- Communication in a system
- Differences between traditional bus and OCB
- Bus architecture
- Basic bus operation
- OCB's issues
- Conclusion

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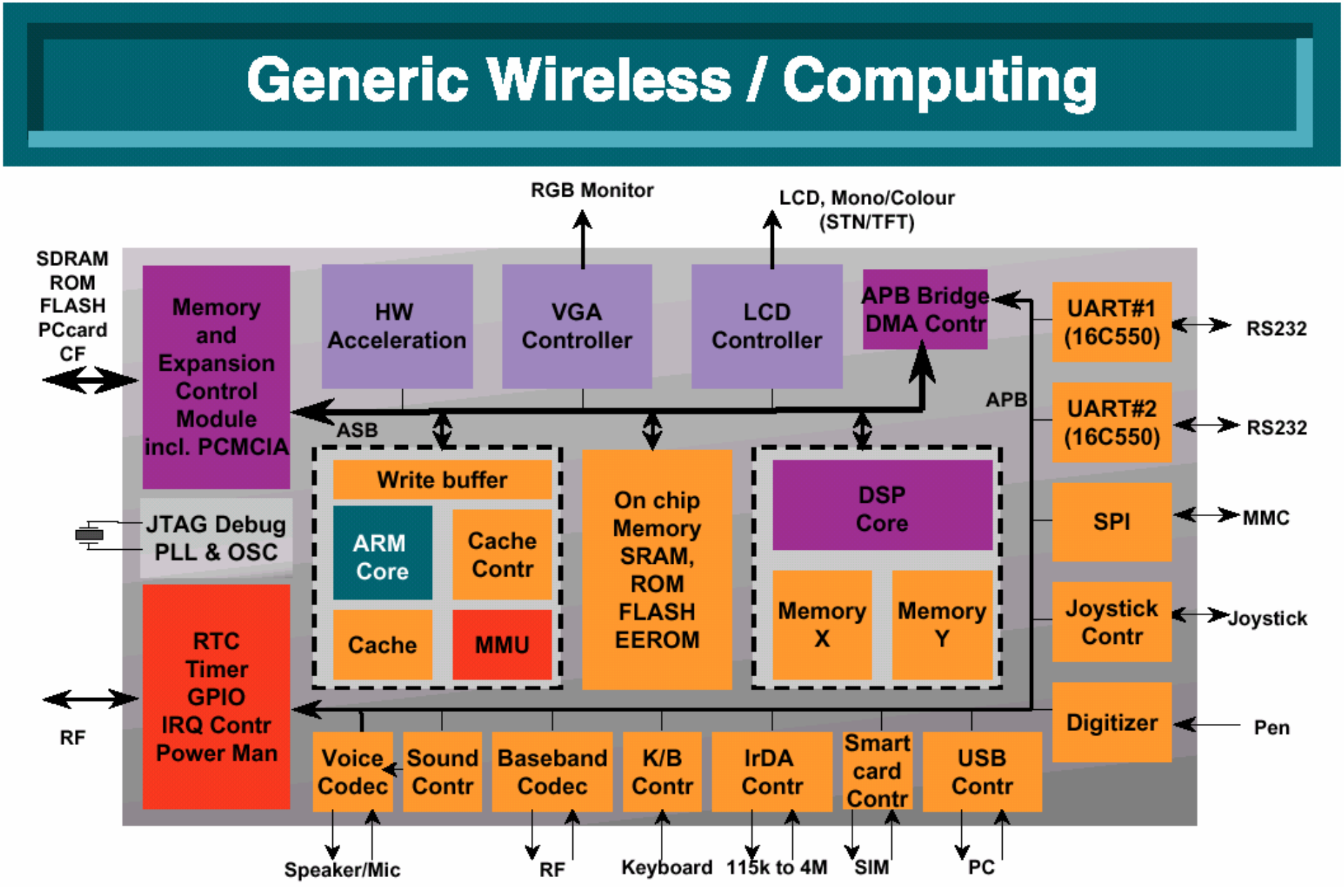
The SoC



Outline

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Communication in a System

- A list of factors that determine system speed: (microcomputer busses)
  - Efficiency and implementation of algorithm
  - Compiler and coding efficiency
  - Multitasking overhead
  - *Data transfer speed*
  - I/O handling speed
- Amdahl's law

✍Microcomputer Buses, R. M. Cram, 1991, Academic Press, Inc.

Communication

- Different views of communication
  - Bus (Abstract)
  - Channel (Point-to-Point)
  - Interconnection (Primitive)
- Definition of a bus (microcomputer busses)
  - A tool designed to interconnect functional blocks of a (macro) computer in a systematic manner. It provides for standardization in *mechanical form*, *electrical specifications*, and *communication protocols* between board-level devices.

Signals in a Bus

- Data
- Address
- Control (most variable part of any given bus type)
  - Multiple masters arbitration
  - Data transfer handshake
  - Interrupt processing
  - Failure handling
- Power?

Outline

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Concept of the Bus

- A group of lines shared for interconnection of the functional modules by a standard interface
  - E.g., ARM AMBA, IBM CoreConnect
- Interconnection structure
  - Point-to-Point
  - On-chip bus
  - On-chip network

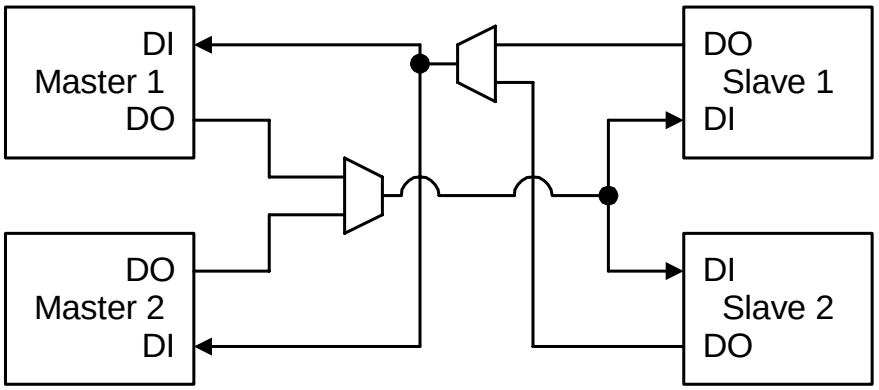
Differences Between Traditional Bus/OCB

- The root: I/O pins are limited and fixed
- The characteristics of a traditional bus
  - Shared I/O
  - Fixed interconnection scheme
  - Fixed timing requirement
  - Dedicated address decoding
- For a OCB
  - Routing resource in target device (e.g. FPGA, ASIC)
  - Bandwidth and latency are important

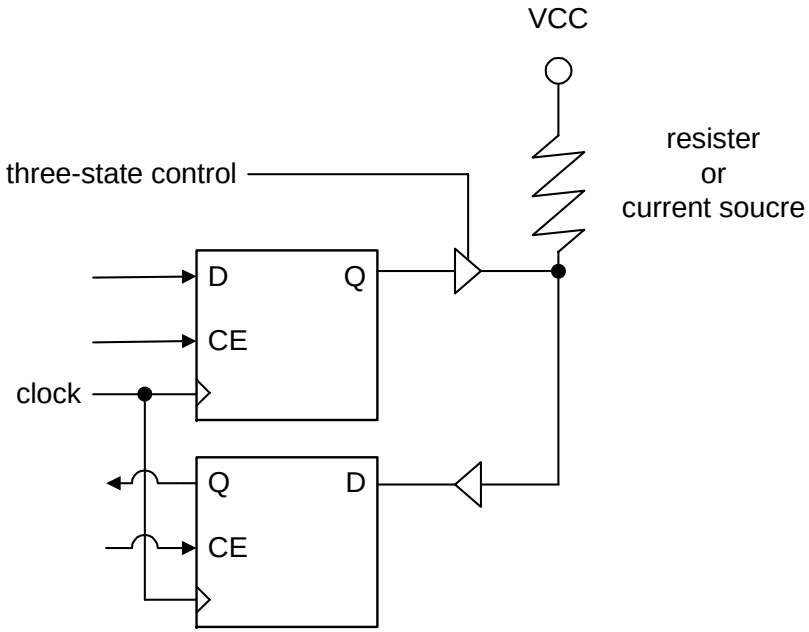
Shared I/O

- Three-state I/O. E.g. multiple masters, input/output
  - Slower than direct interconnection
  - Limited by bus keeper or quality of routing resource in the target device
  - Solution in OCB: multiplexer logic interconnection
  - Xilinx design guideline: We recommend using multiplexer-based buses when designing for reuse since they are *technology-independent* and more portable.
- Multiplexed functional I/O. E.g. address/Data.
  - Need more time to transfer the same amount of data
  - Solution in OCB: separate buses

Physical View of Shared I/O



Multiplexer-based buses



Three-state I/O

Physical Constraints

- Fixed Interconnection Scheme
  - Traditional buses usually routed across a standard backplane
  - OCB allowed a variable interconnection scheme that can be defined by the system integrator at the "*tool level*"
- Fixed Timing Requirement
  - Traditional buses have fixed timing requirements:
    - They are both tested as sub-assemblies
    - They have highly capacitive and inductive loads
    - They are designed for the *worst-case* operating conditions when unknown bus modules are connected together
  - OCB has a variable timing specification that
    - Can be enforced by place & route tools (tool level)
    - Usually does not specify absolute timing
    - Possibly only specifies a single timing specification（WISHBONE, Silicore）

Address Decoding

- Standard microcomputer buses usually use the full address decoding technique
  - That's because the interconnection method does not allow the creation of any new signals on the interface
- OCB can only use partial address decoding
  - Higher speed address decoder
  - Less redundant address decoding logic
  - Integrator must define part of the address decoder logic for each IP core (disadvantage)

Outline

- Communication in a system
- Differences between traditional bus and OCB
- ***Bus architecture***
- Basic bus operation
- OCB's issues
- Conclusion: OCB's future

Bus Components

- Switch or node
  - arbitration,routing
- Converter or bridge (type converter)
  - from one protocol to another
- Size converter
  - buffering capacity

Bus Transaction

- Bus cycle
  - one bus clock period
- Bus transfer
  - read or write operation, 1 or more bus cycles
  - terminated by a completion response from the addressed slave
- Burst operation
  - one or more data transaction, initiated by a bus master

Bus Transfer

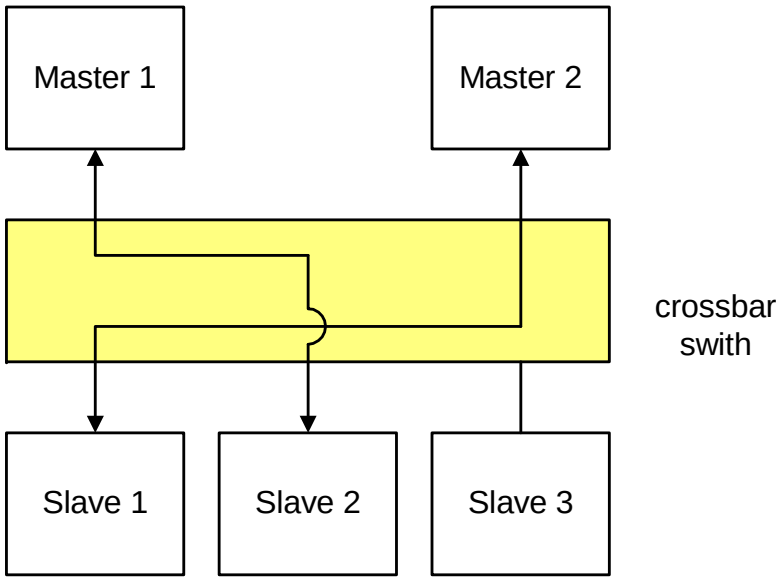
- A means to transfer data on the shared communication lines between VCs
- Protocol: guarantee the correct transfer
  - request arbiter to use bus
  - request sender to send data → sender ACK →send data → receiver ack to receipt
  - if error, re-send
  - release bus
- Transfer modes
  - read or write
  - asynchronous or synchronous
  - transfer size 8, 16, 32, 64, 128 bits
  - transfer operations

Bus Signals

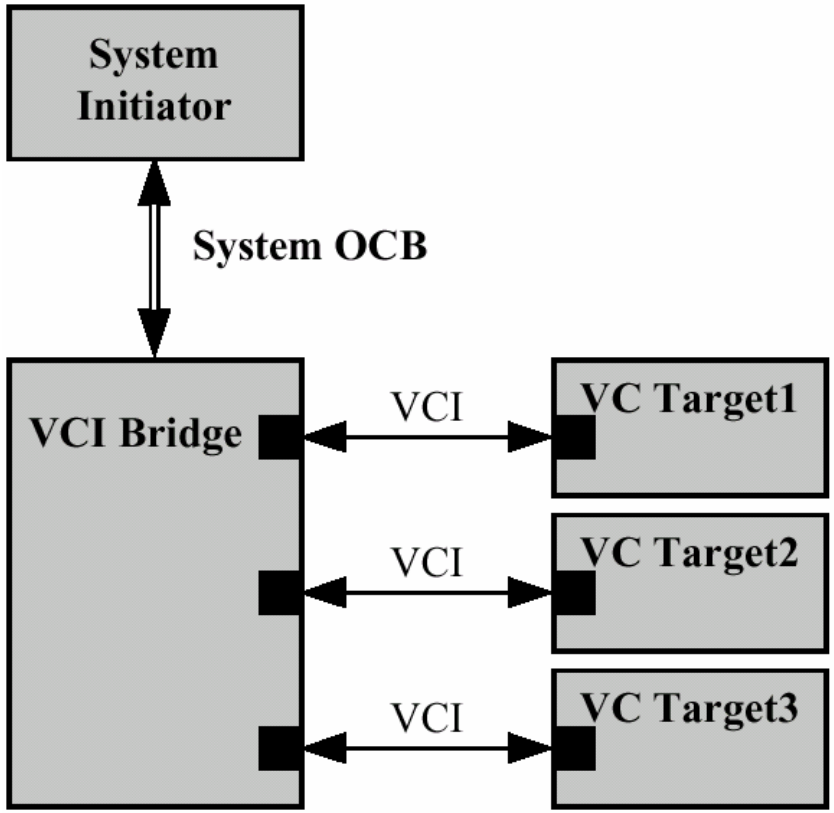
- Address and data
- Interface controls
- Arbitration
- Interrupt
- Error reporting
- System level
- Test/Boundary scan
- Others

Bus topology

- A single bus
- Multiple buses
- Crossbar switch
- No shared bus (star topology)



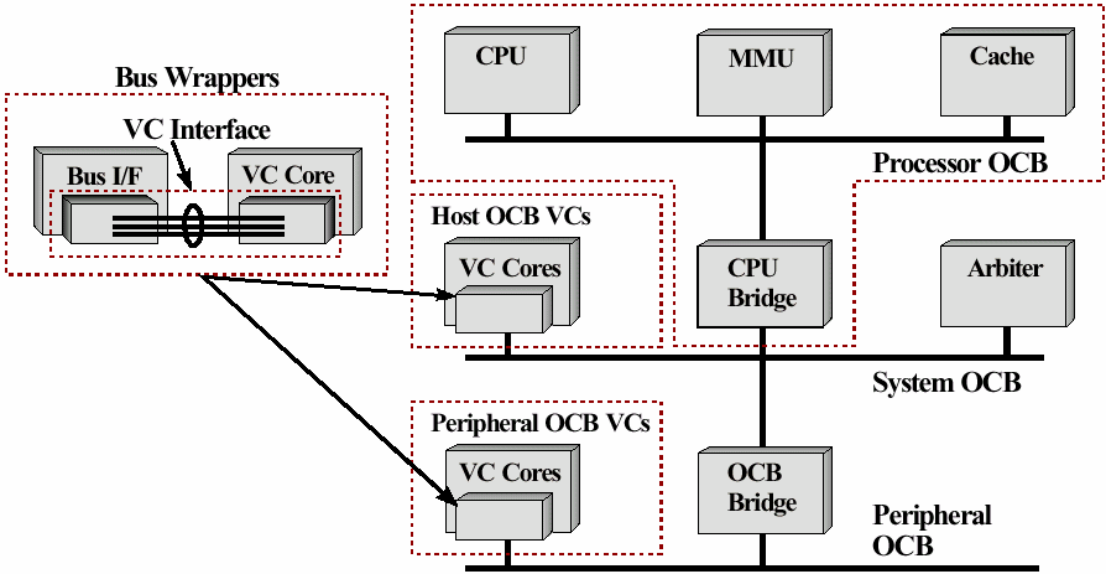
Crossbar switch



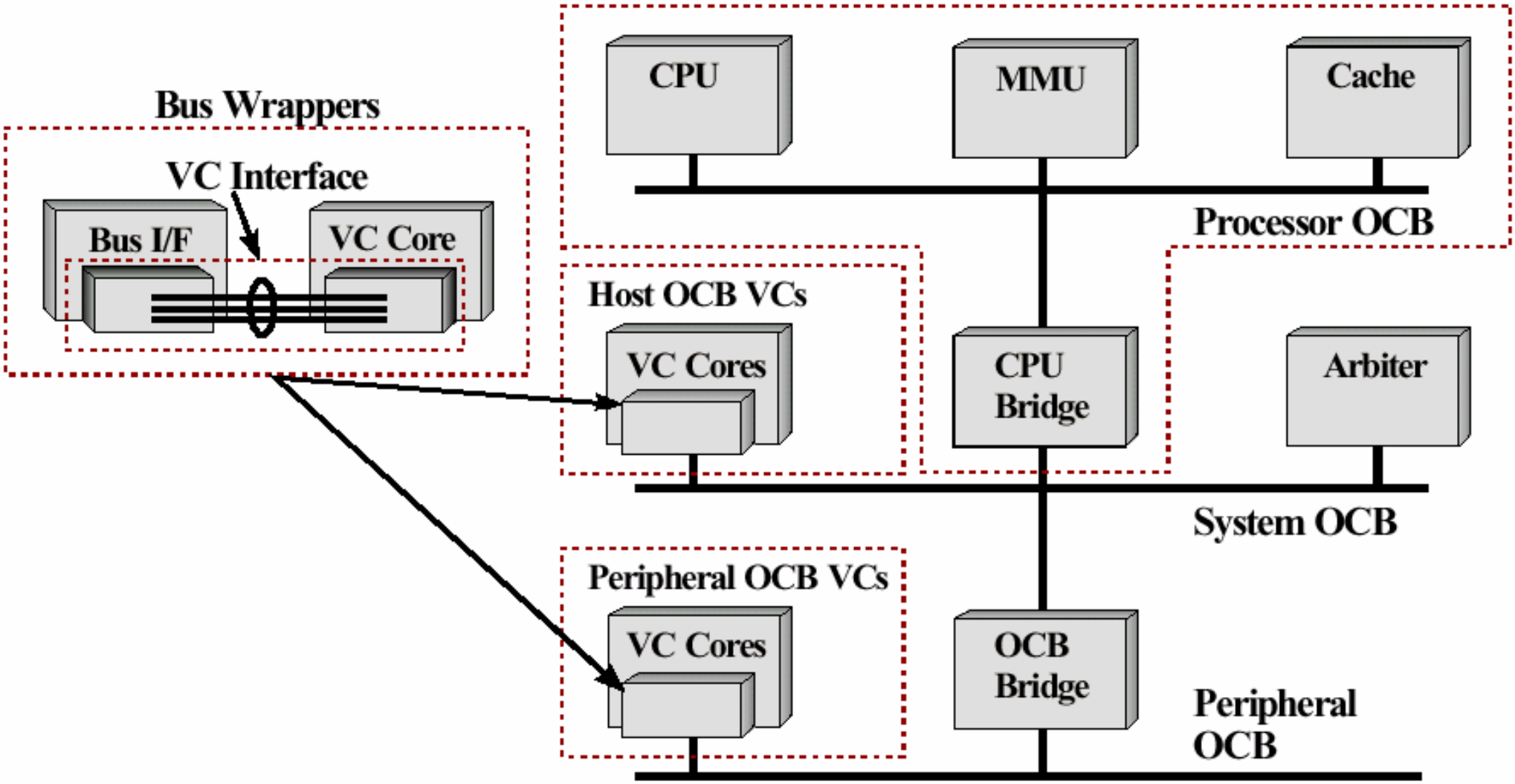
VCI with star topology

Bus Hierarchy

- The structure of multiple buses within a system, organized by bandwidth
- Local processor bus
  - highly processor-specific
  - processor, cache, MMU, coprocessor
- System bus (backbone)
  - RISC processor, DSP, DMA (masters)
  - Memory, high resolution LCD peripheral
- Peripheral bus
  - Components with other design considerations (power, gate count, etc.)
  - Bridge is the only bus master



Multiple buses - Hierarchical Bus (VSIA)

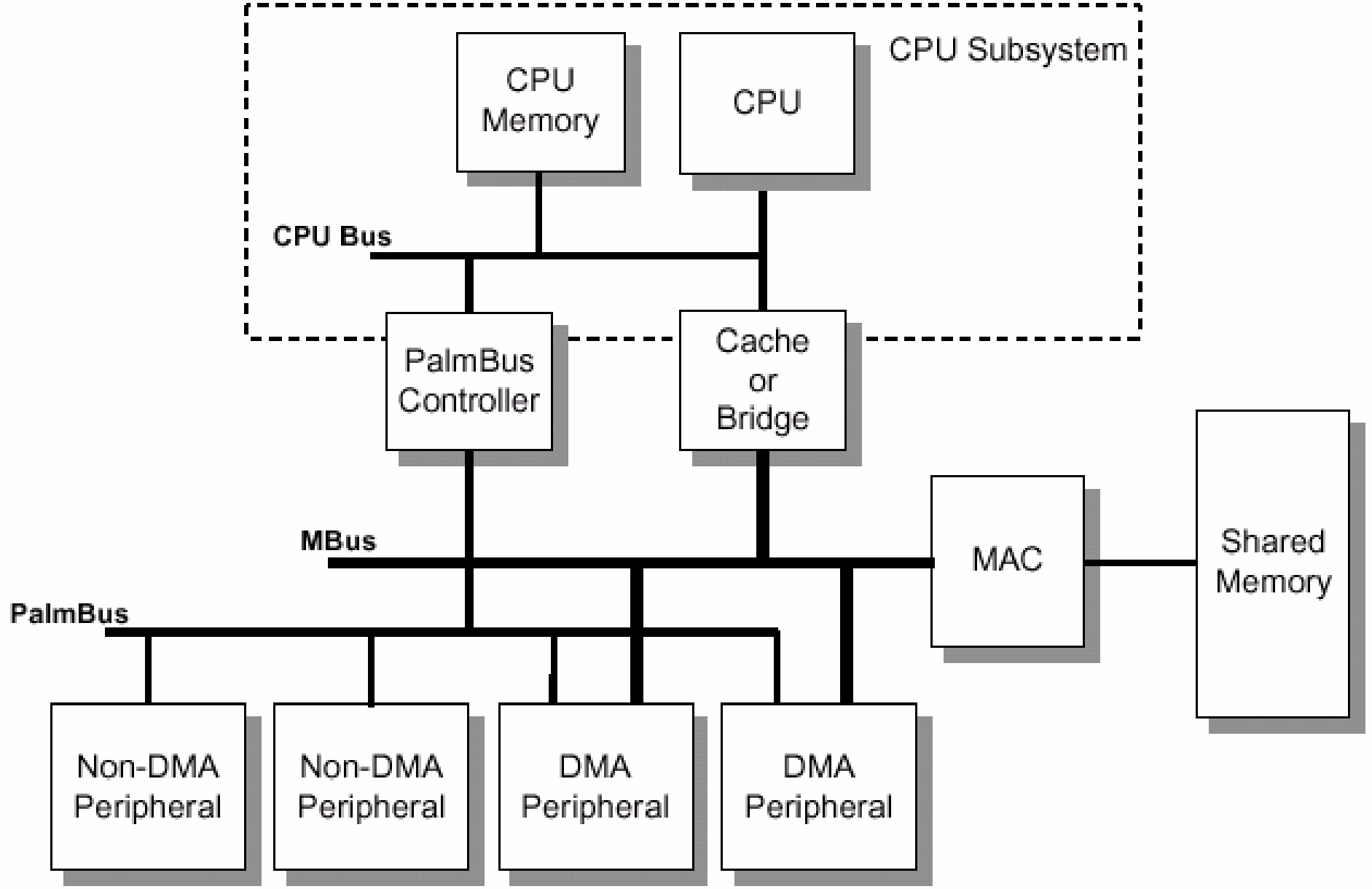


Characteristics of Hierarchical Bus

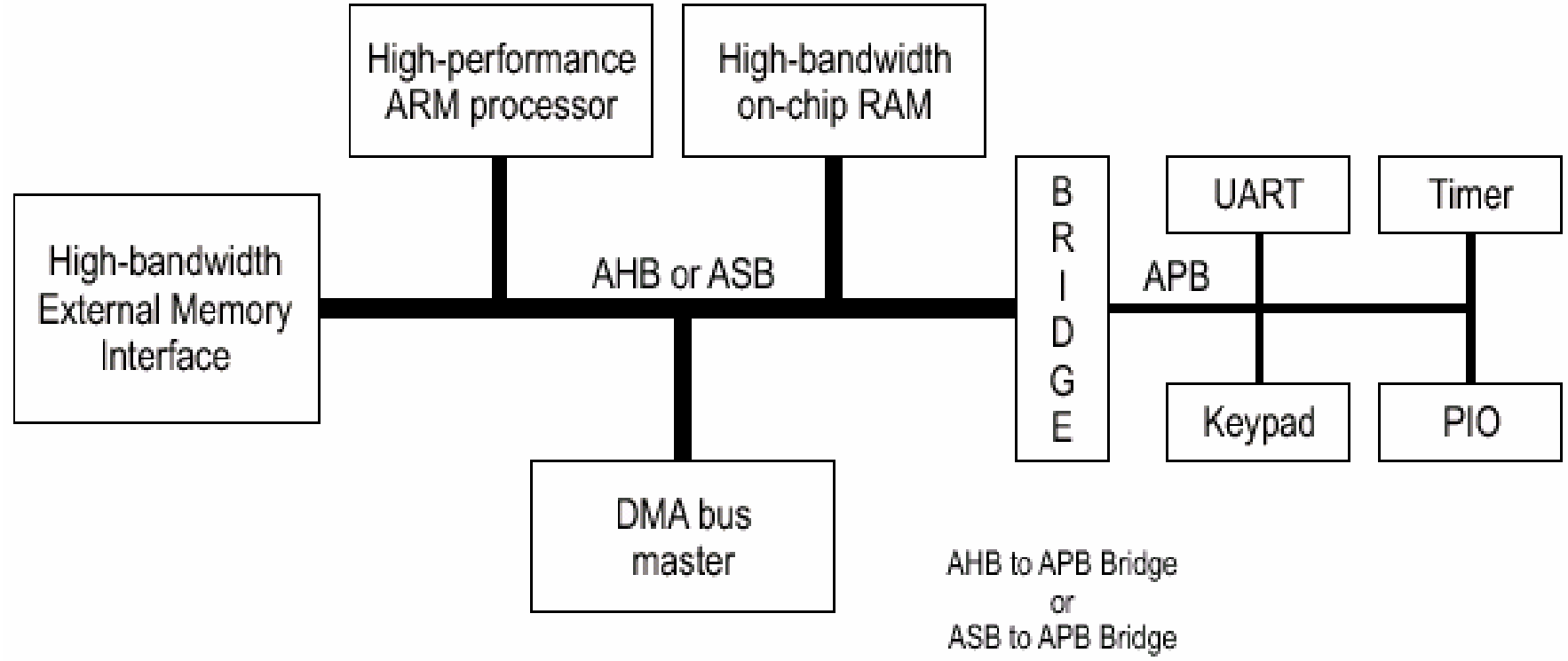
- Processor bus: tailored to processor's attributes and memory system
- System bus and peripheral bus

System Bus	Peripheral Bus
Multiple bus master	Single bus master
Pipelined operation	Non-pipelined operation
Burst transfers	Single transfer only
Variable transfer duration	Fixed transfer duration
Split transactions	No split transactions
Cache support	No cache support
Error codes/timeout	No timeout support
Timing analysis	Timing ensured by protocol

Multiple buses - Parallel Bus (PalmBus & MBus)



Multiple Bus - Alternative Bus (AMBA)



AMBA AHB

* High performance
* Pipelined operation
* Multiple bus masters
* Burst transfers
* Split transactions

AMBA ASB

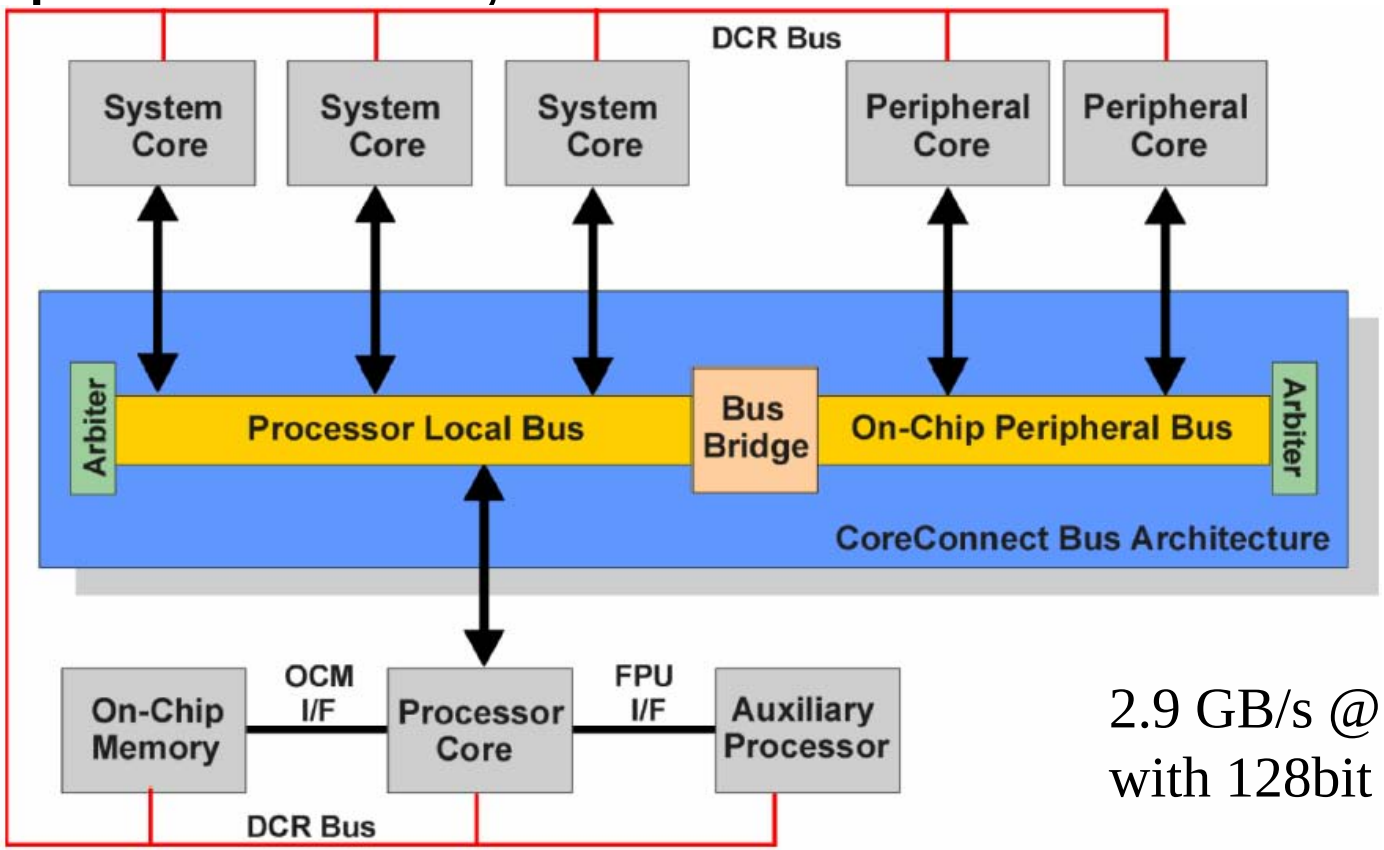
* High performance
* Pipelined operation
* Multiple bus masters

AMBA APB

* Low power
* Latched address and control
* Simple interface
* Suitable for many peripherals

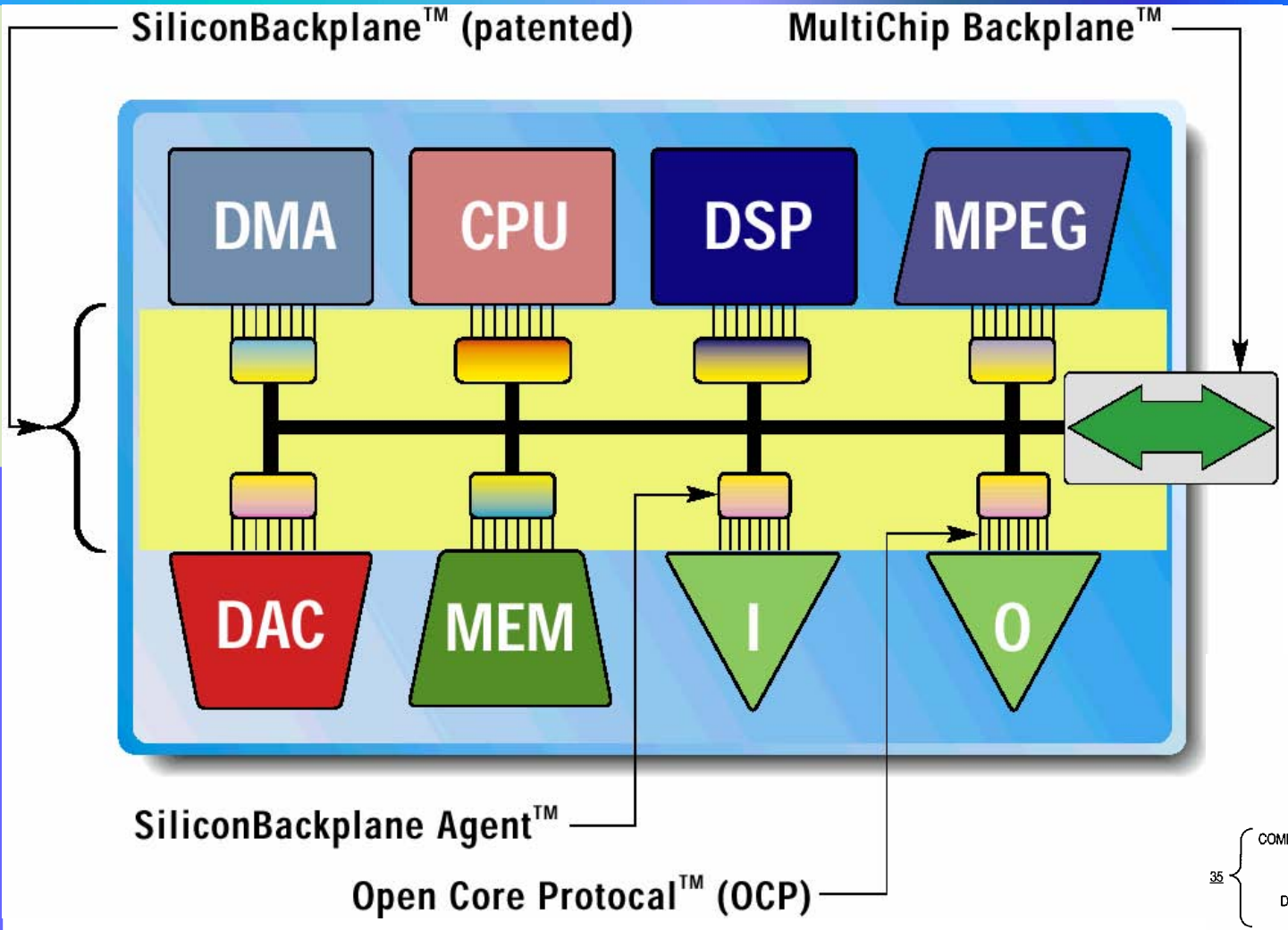
Multiple Bus - Extra Control Bus (IBM CoreConect)

- Device Control Bus (DCR)
  - Provides fully synchronous movement of GPR data between CPU and slave logic
- High performance, well documented

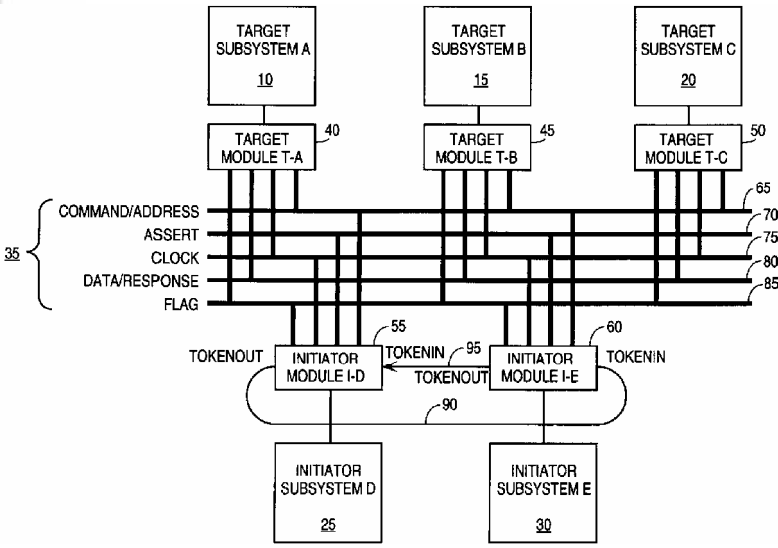


2.9 GB/s @183 MHz with 128bit width

Automated Bandwidth Allocation Bus System - SiliconBackplane of Sonics

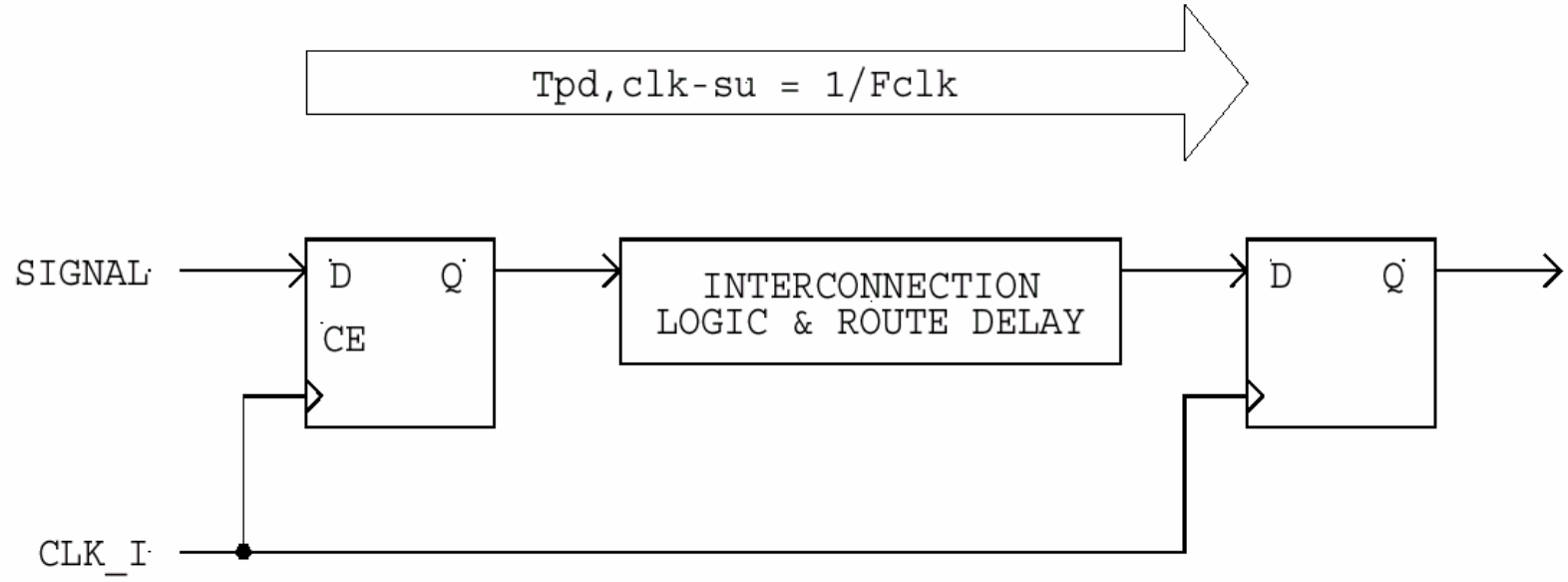


Data transfer rates :
50MByte/s ~ 4GByte/s



Tool Based Bus - WISHBONE of Silicore

- Define an interface specification rather than a bus specification
  - Simple handshaking protocol
- A single timing specification
  - Time delay between a positive clock edge on [CLK_I] to the setup on a stage further down the logical signal path
  - Timing is guaranteed by place & route tool



Other Buses Proposed in VSIA OCB DWG

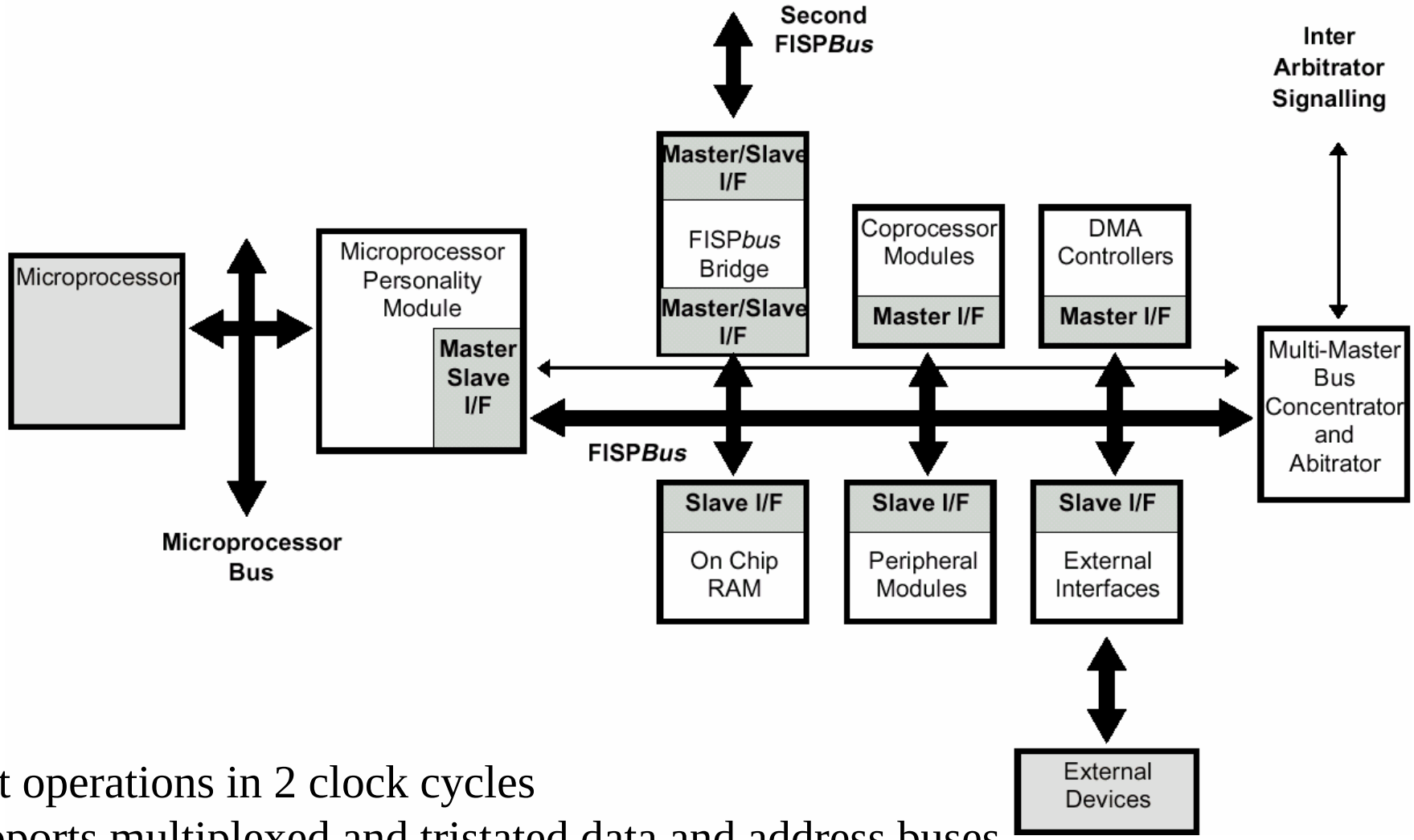
- Model-Year Architecture (MYA)
  - Lockheed Martin Advanced Technology Laboratories
  - Specify interface protocol (Standard Virtual Interface Approach)
- General purpose Bus (G-bus) - Toshiba
  - Three levels of internal busses: X bus, G bus and IM bus
  - Like VSIA's hierarchical bus
  - Adds one external bus interface on G bus for external memory

Other Buses Proposed in VSIA OCB DWG

- PCI as an On-Chip Bus (Virtual Chips Products)
  - Phoenix Technologies Ltd. (Insilicon)
  - Advantage:
    - Widely used
    - Power management features
    - BIOS, O/S and driver support
    - Well supported by simulation models, verification suites and test methods
    - Royalties free
  - Disadvantage:
    - Relatively high power requirements
    - Gate count (7-15K gates)
    - Multiplexed, tri-state address and data lines,
      - Splitting the tri-states is trivial

Other Buses Proposed in VSIA OCB DWG

- FISP bus (GF-FISP bus) - Mentor Graphics



😐 Fast operations in 2 clock cycles

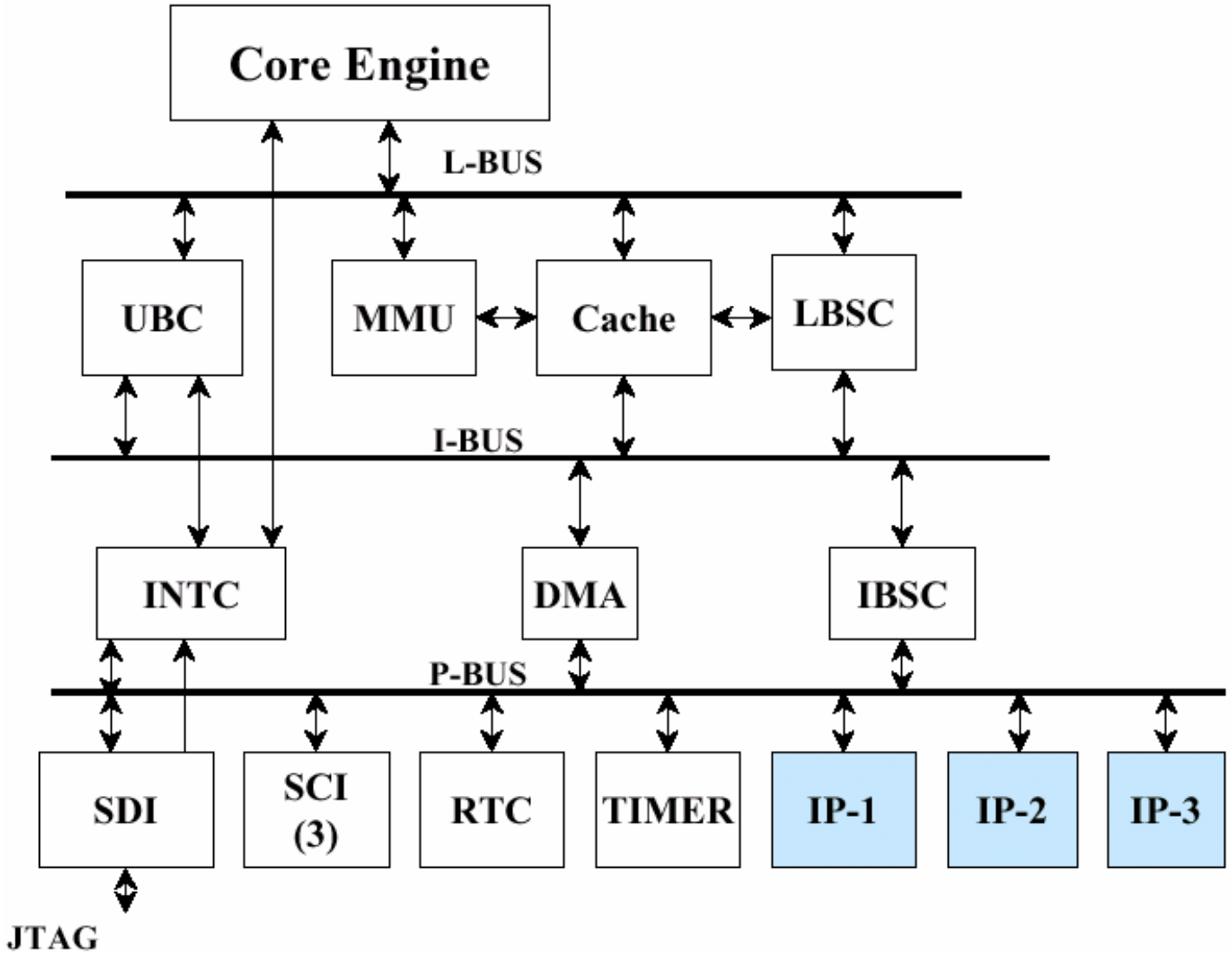
😐 Supports multiplexed and tristated data and address buses

Other Buses Proposed in VSIA OCB DWG

- PIBUS Standard - SGS-Thomson
  - Features
    - Existing open standard (licensing agreement)
    - Several PIBUS Implementations (Sparc, MIPS, ST20)
    - AMBA and PIBUS are largely equivalent at transaction level
  - Commercial Issues
    - Lack of control over standard
    - Uncertainty over PIBUS support
  - Conclusion in the present
    - Define a set of virtual component Interfaces
    - Protocols independent of bus
    - Timing guidelines

Other Buses Proposed in VSIA OCB DWG

- Hitachi Super H Bus Interface



Summary - OCB Architecture

- How to extract other OCBs' features?
- Core interface: bus-centric or core-centric?
  - Bus-centric: AMBA, FISP bus, ...
  - Core-centric: VCI, OCP, WISHBONE
- Design methodology
  - Manual design (bus view)
  - Automated busing system (channel view)
  - Tool based bus (interconnection view)

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Bus Transfer - Data Format

- Endianness
  - Big-endian: The most significant byte is first.
    - (msb)()()(lsb) for 32 bits
  - Little-endian: The least significant byte is first.
    - (lsb)()()(msb) for 32 bits
- Data bus width and data cell width
  - Controlled by byte enable/mask
- Others
  - address width, data width

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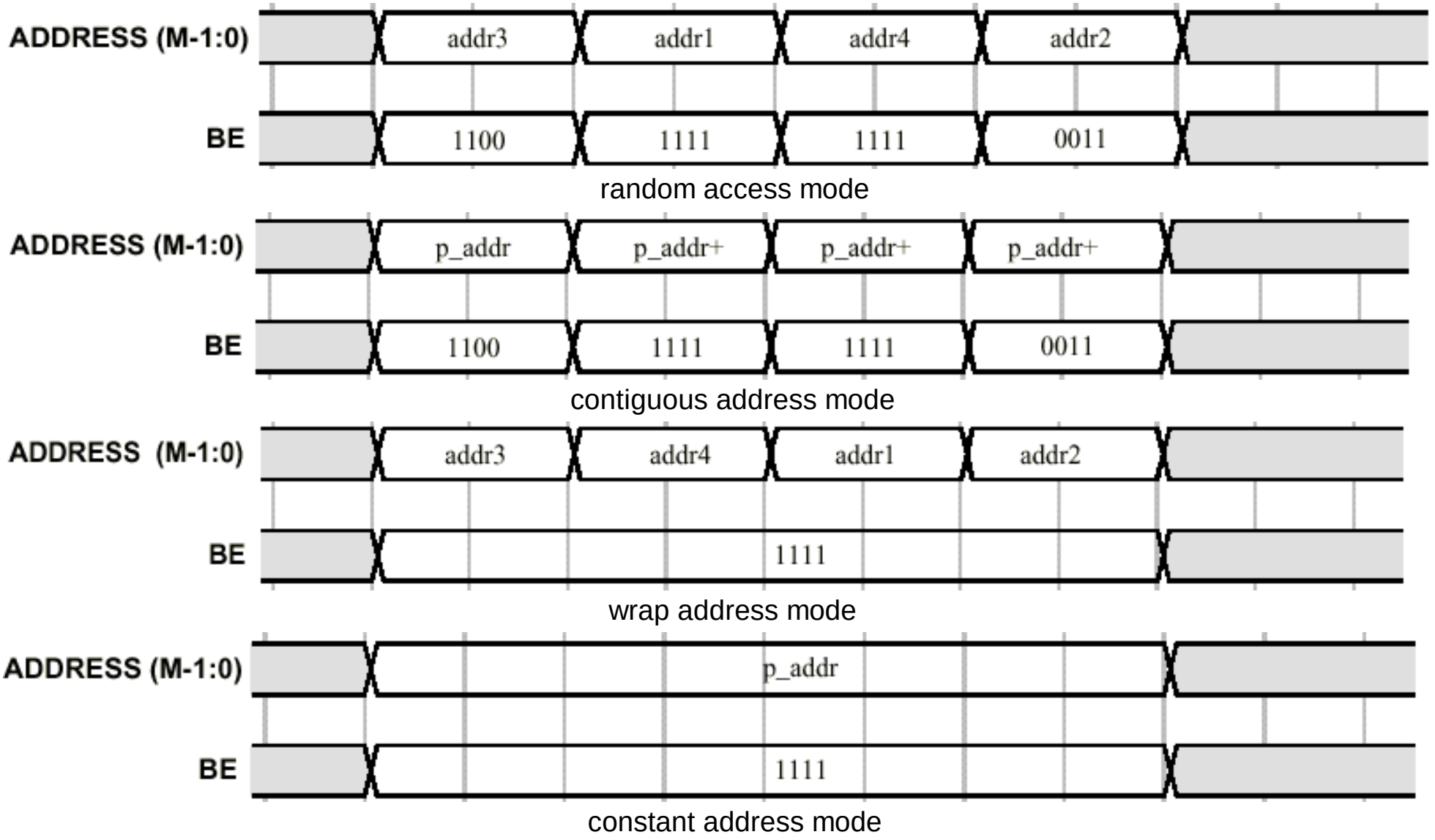
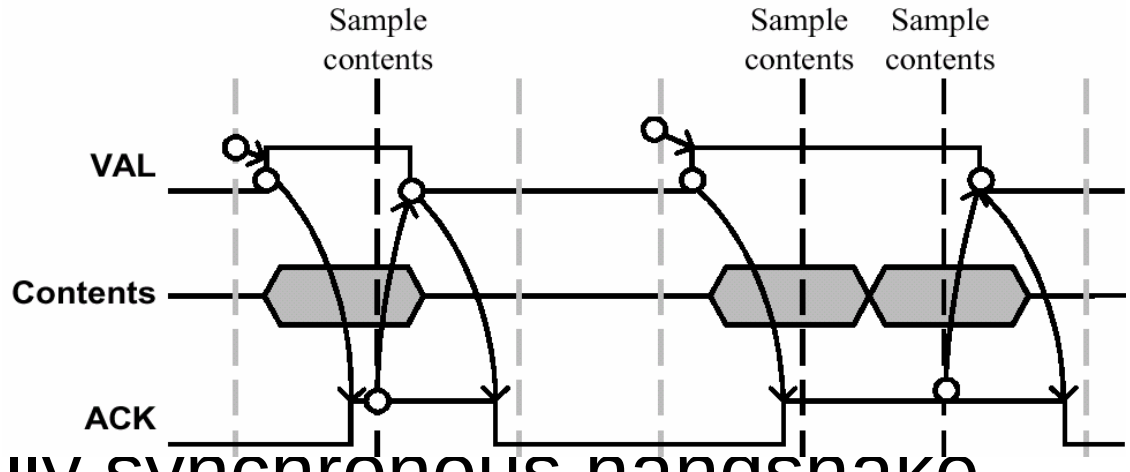
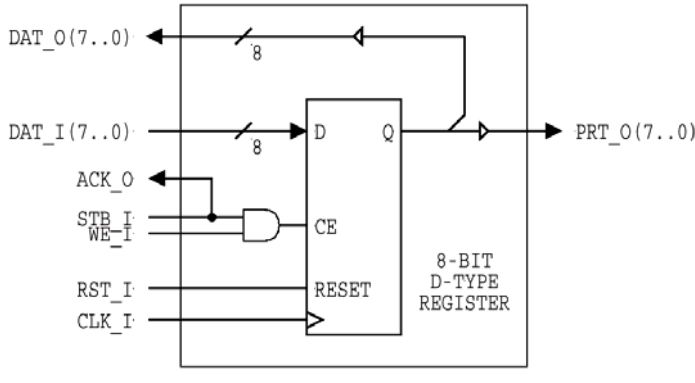
Bus Transfer - Addressing Mode



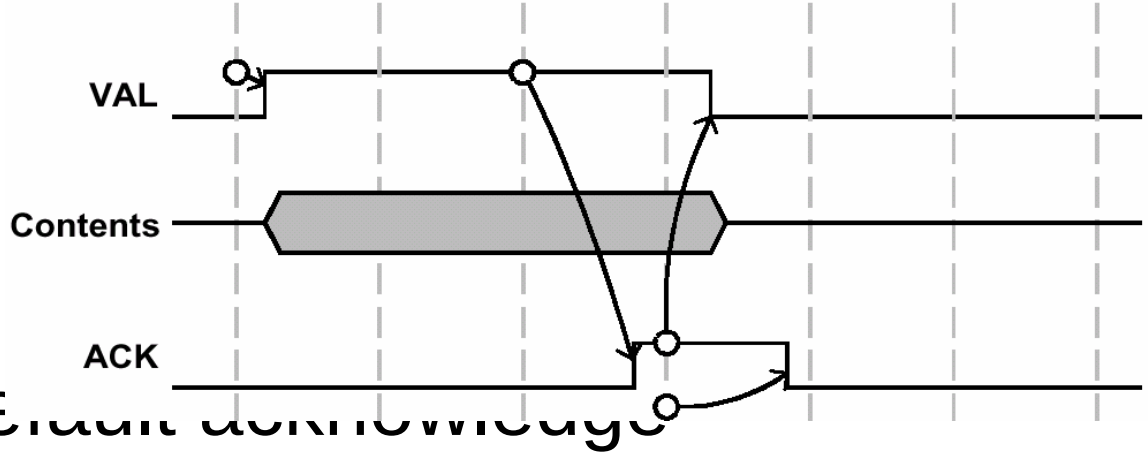
Basic Control Protocol: Handshake

- Asynchronous ACK





- Fully synchronous handshake

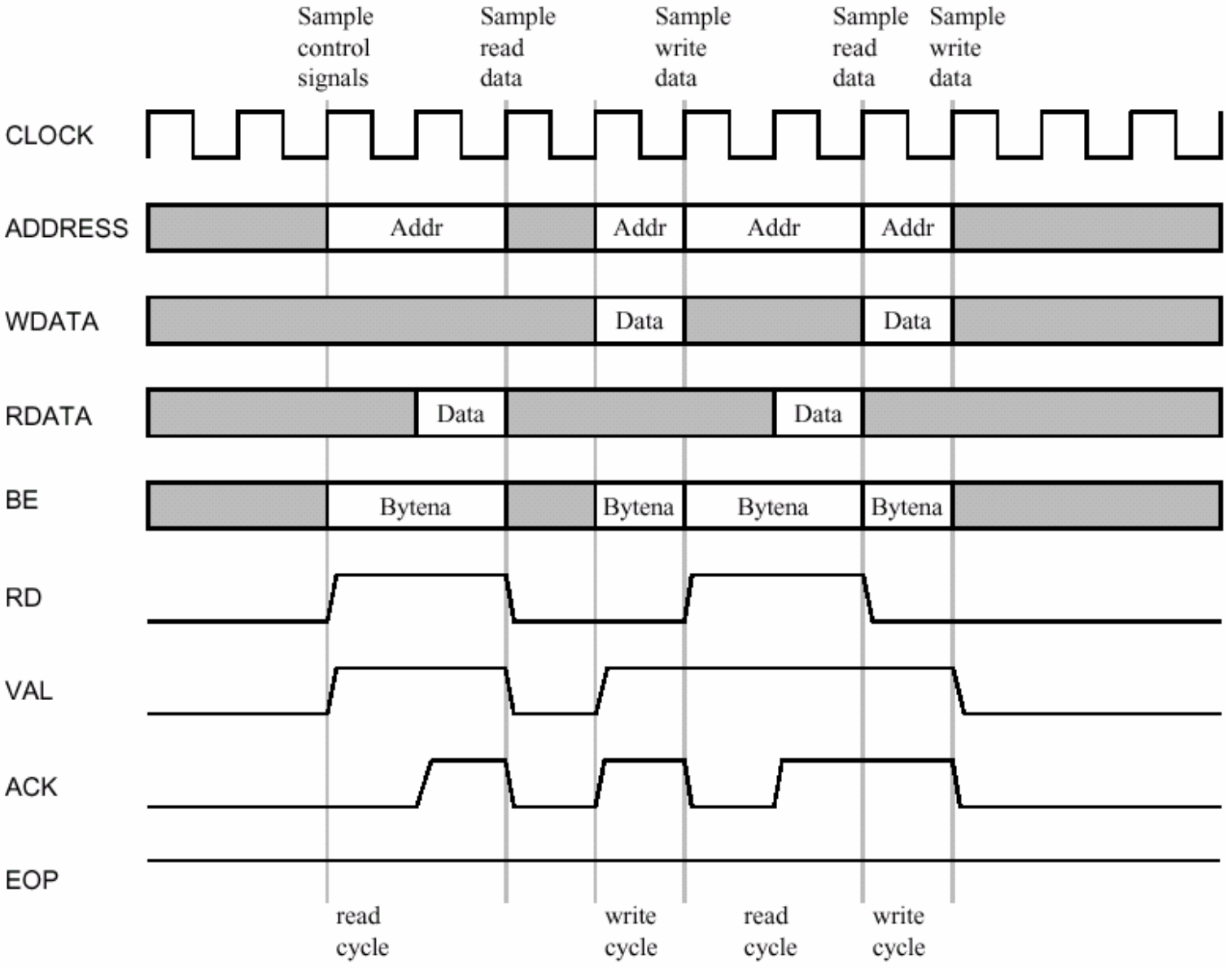


ACK late by 2 cycles

- Default acknowledge

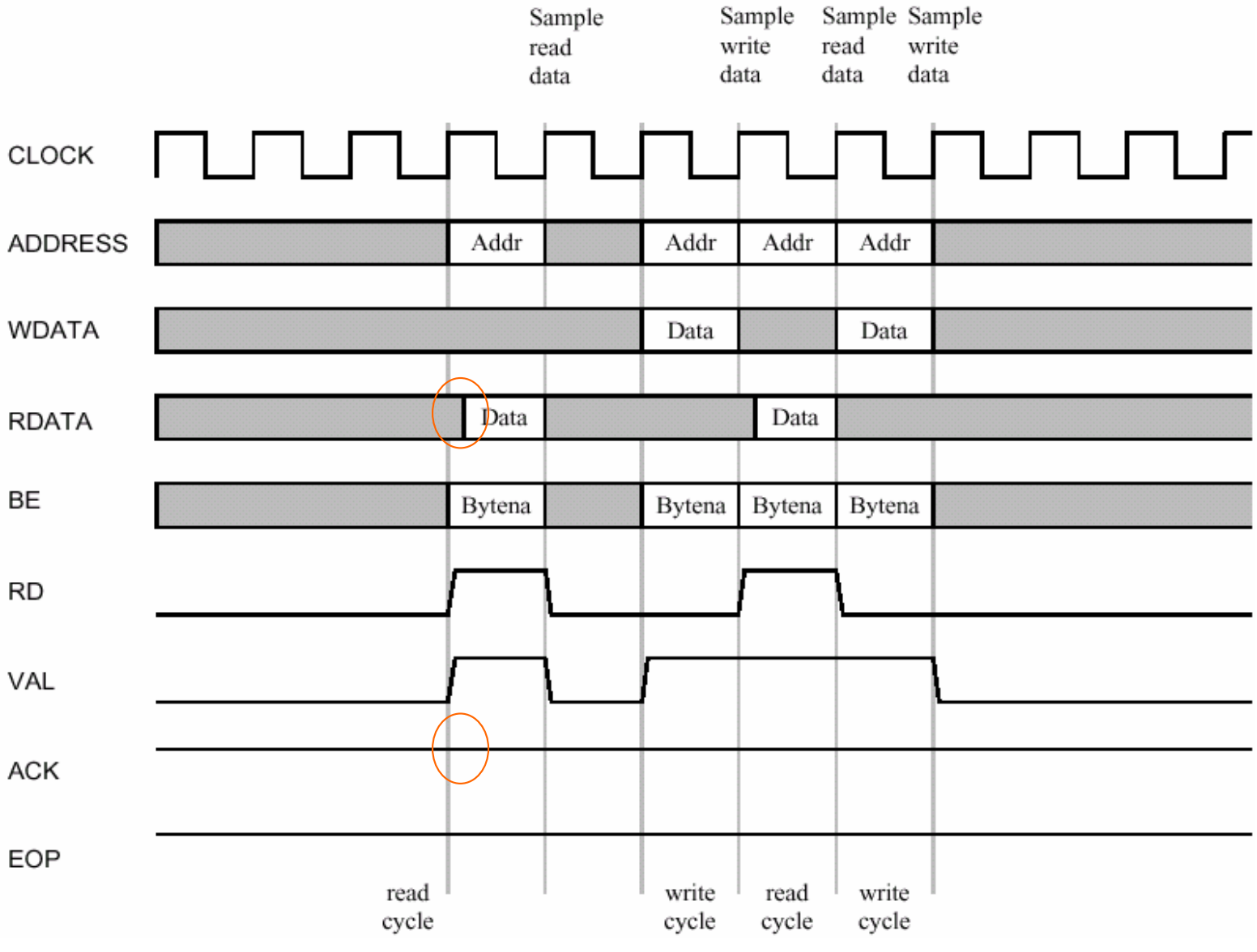
✍Synchronous: a signal is changed/sampled when rising edge of the clock

Basic Transfer Cycle - Single READ/WRITES



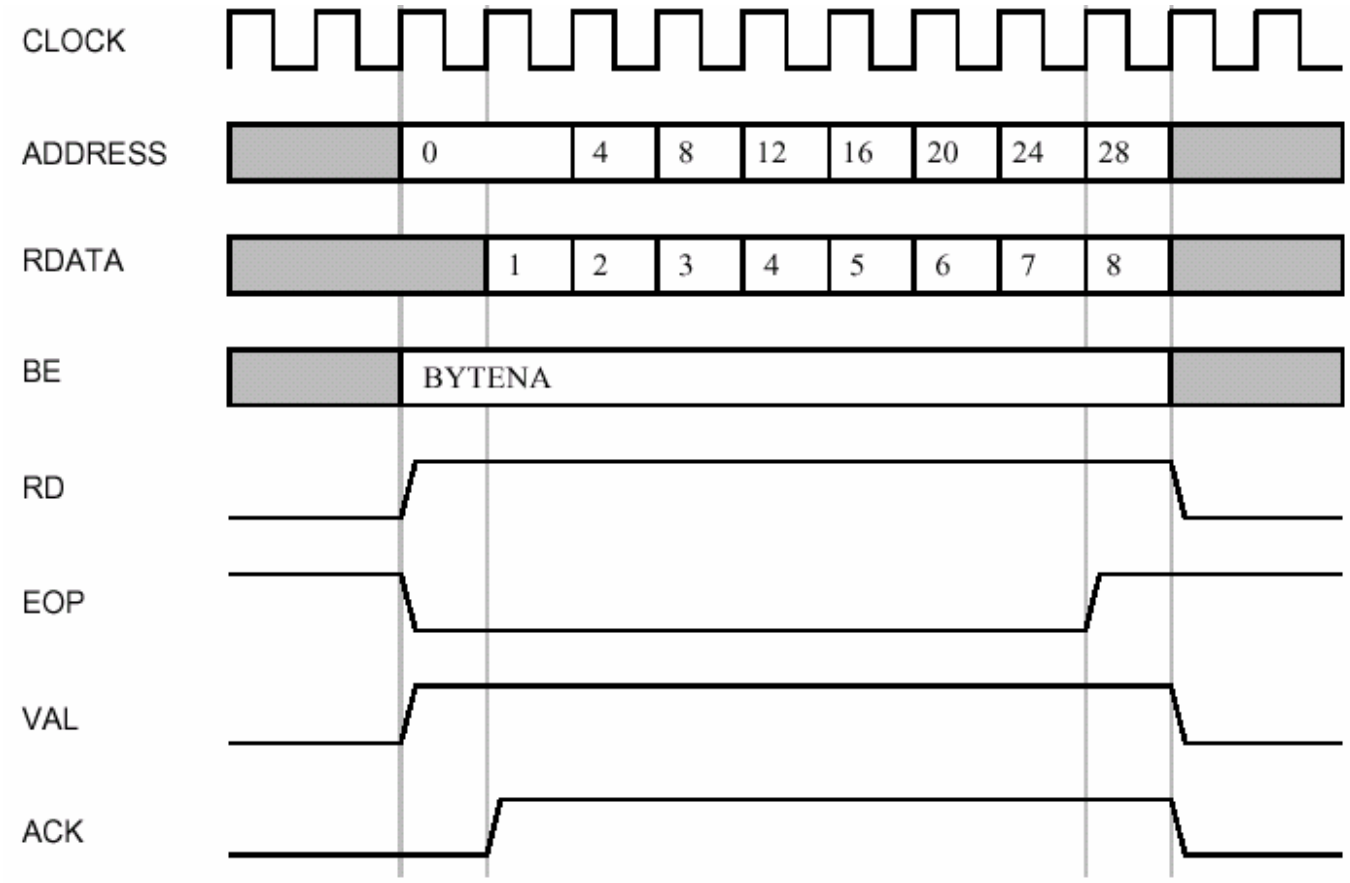
✍See also OCB 2 1.0 PVCI Read and Write

Basic Transfer Cycle - Single READ/WRITE with Default Ack



✍See also OCB 2 1.0 PVCI Read and Write with default acknowledge

Basic Transfer Cycle - Burst Mode



- Data transfer at
  - every cycle
  - every n cycles
- Addressing
  - Alignment

✍See also OCB 2 1.0 PVCI burst read

Other Bus Transfer Cycles

- Data cycle
  - (Multiple) Split transactions
  - DMA transfers
  - Locked transfer
  - Broadcast transfer
  - Cache line transfers
  - Packet chain transfer
  - Transfer with retry
- Arbitration cycle
  - Overlapped arbitration

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- ***OCB's issues***
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OCB's issues

- The development of OCB
  - Topology
  - Control mechanism: bus protocol, arbitration
  - Core interface: open standards or other in-house spec.
  - Bus interrupt/error handling
  - Test-bus architecture
  - Buffer
- Target device (FPGA or ASIC) Routing resource
- Supported tools and methodology

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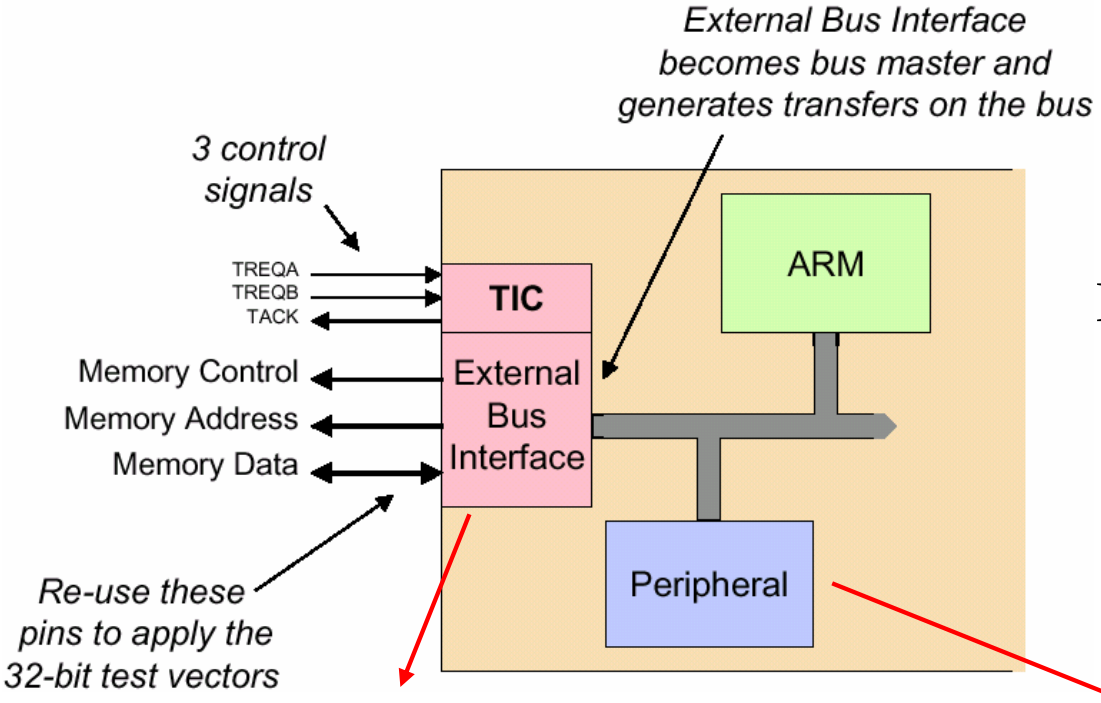
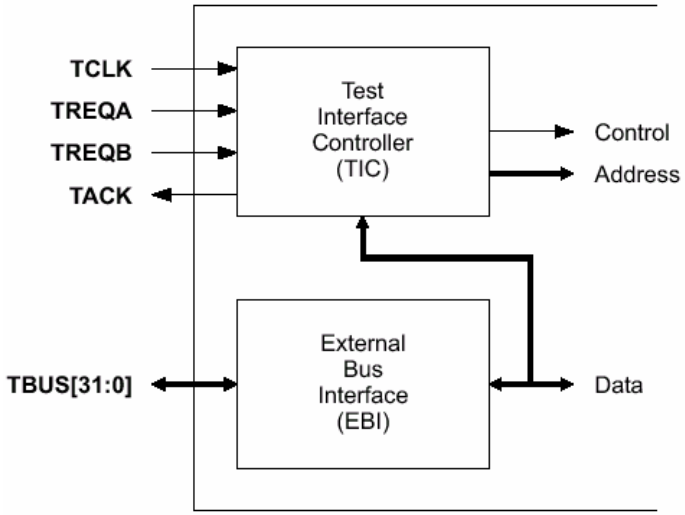
Bus Related Standard

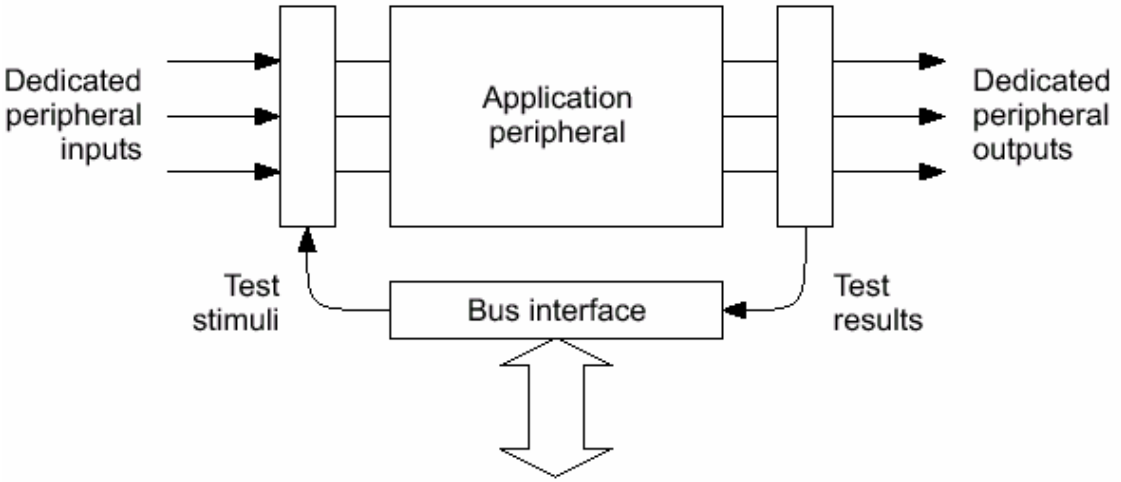
- Core protocol standard
  - OCB 2 1.0, Virtual Component Interface (VCI) Standard, Released March 2000
  - OCP
  - WISHBONE
- Bus protocol standard (show the table)
- Other standard
  - OCB 1 1.0, On-Chip Bus Attributes, Released August 1998
  - SLD 1 1.0, System-Level Interface Behavioral Documentation Standard, Released March 2000
  - OCB 2 Appendix, specification of the Transaction Language (will be included in Ver. 2.0)

OCB for Testability - Isolate the Core



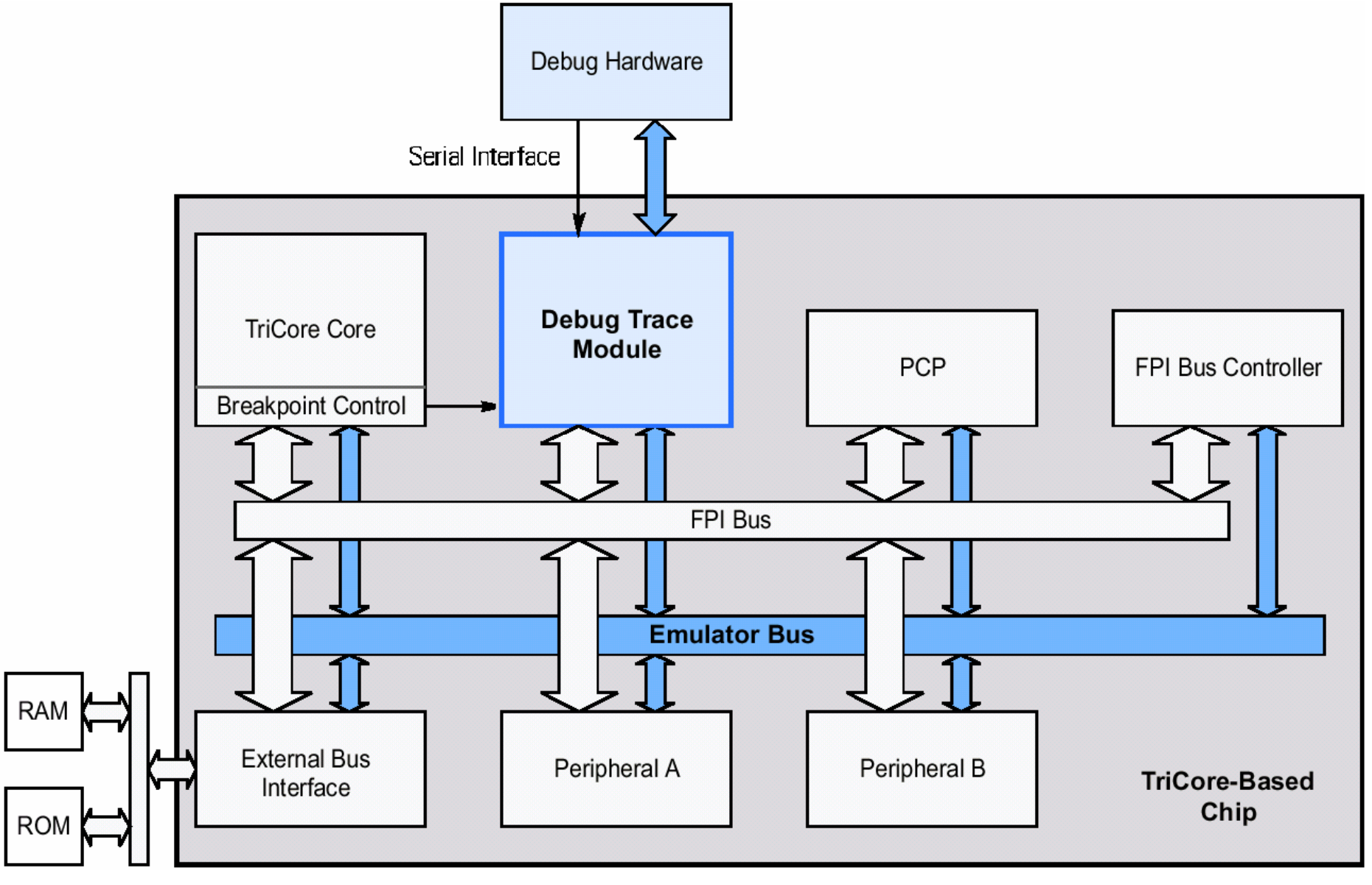
Isolation: not rely on the interaction of any other system element





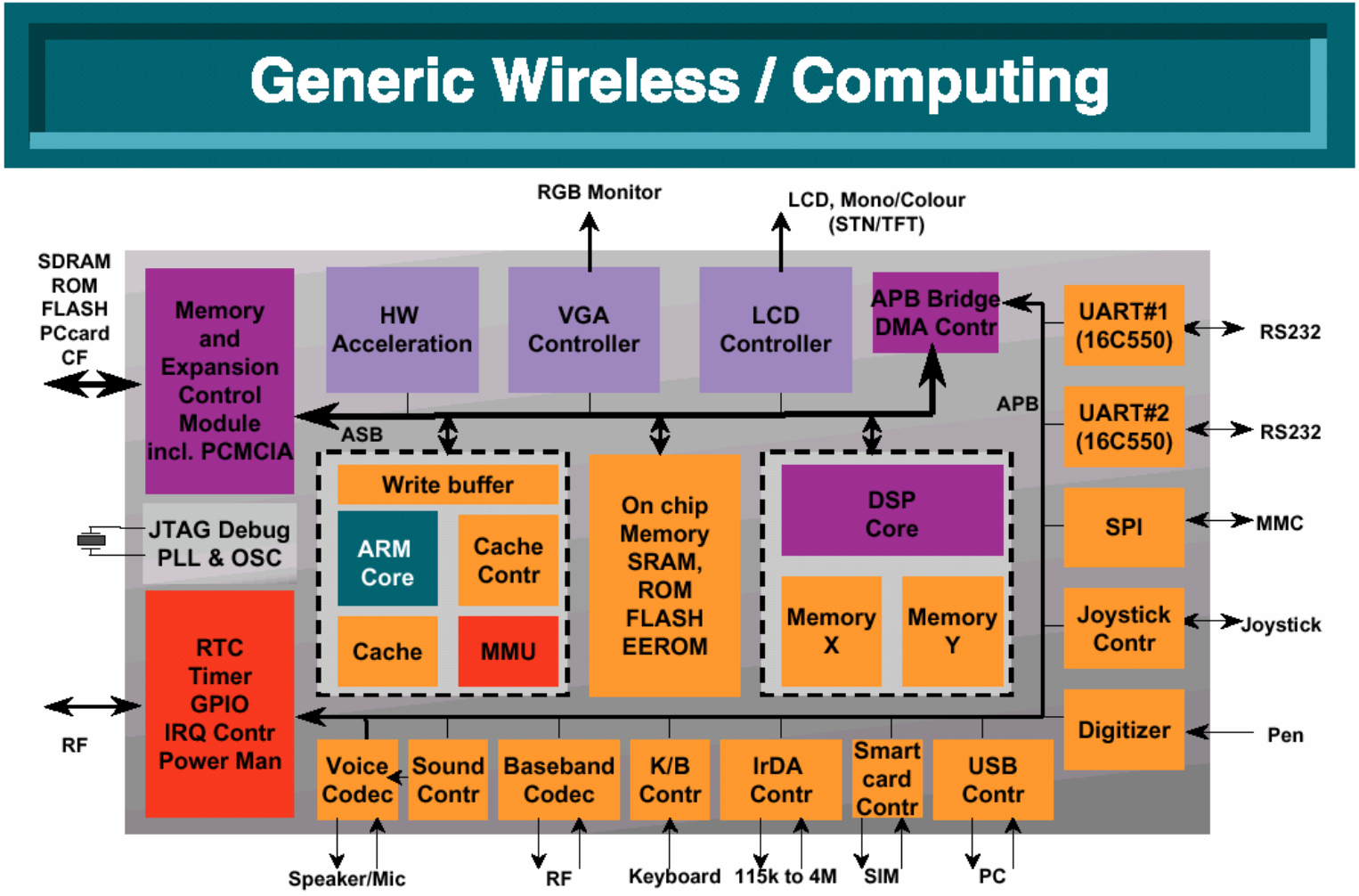
Example from AMBA

OCB for Testability During Simulation



✍Example from FPI bus, Infineon TriCore Architecture Overview_archive.pdf

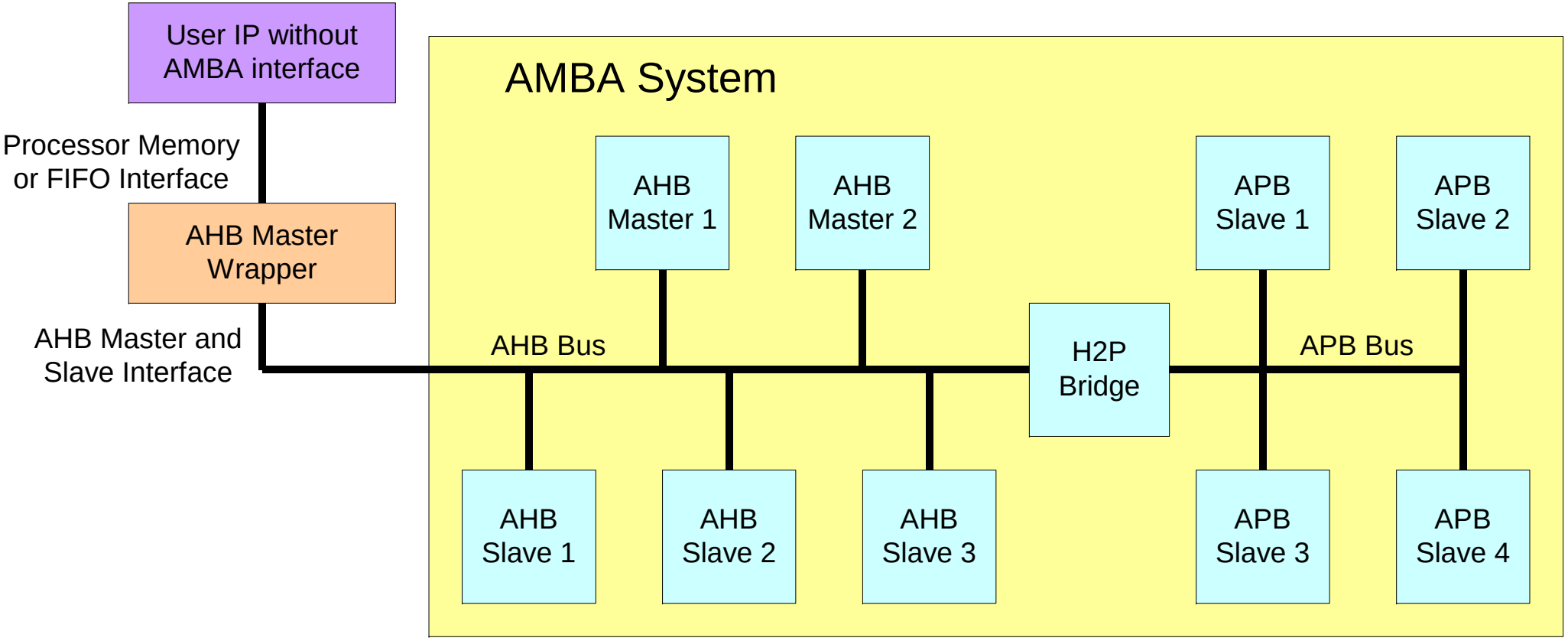
How to Design/Integrate a System?



- How to select a core's interface?
- How to select a bus architecture?
- How to determine each elements in a bus
  - arbiter
  - buffer

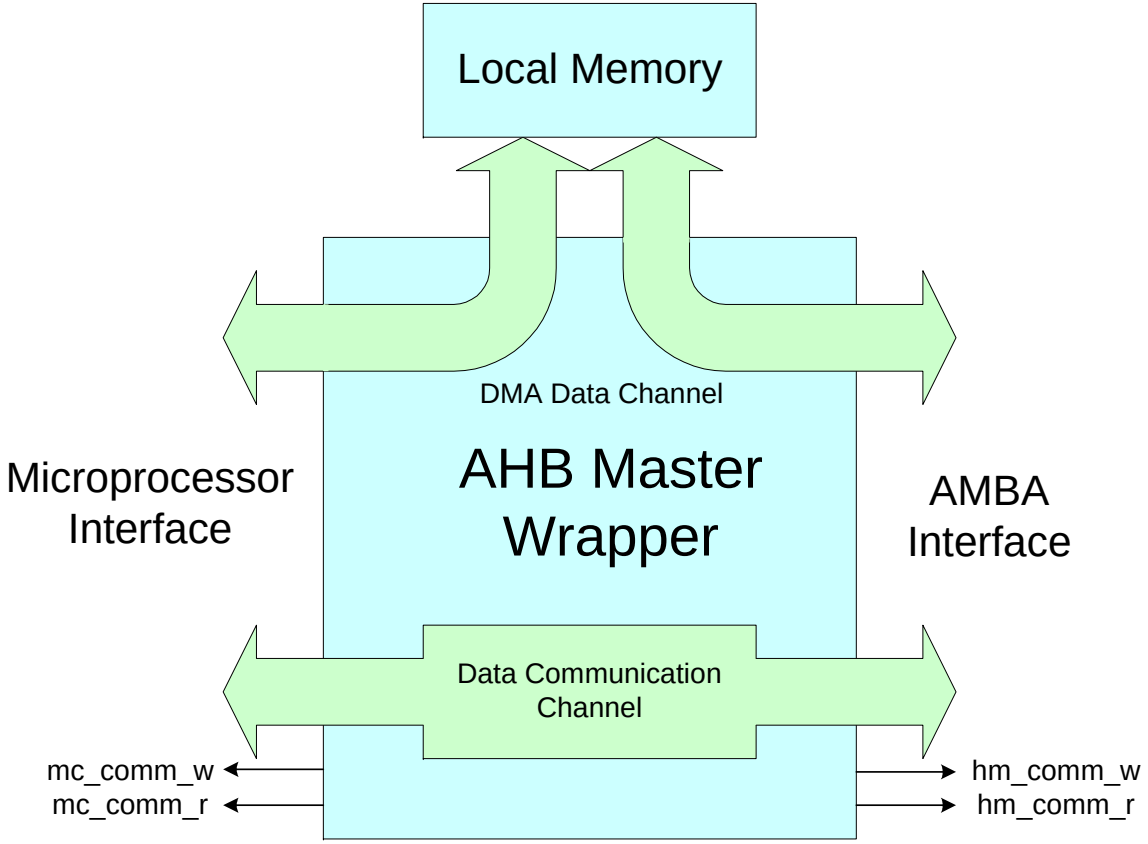
How to test?

Integrate IP Without AMBA Interface



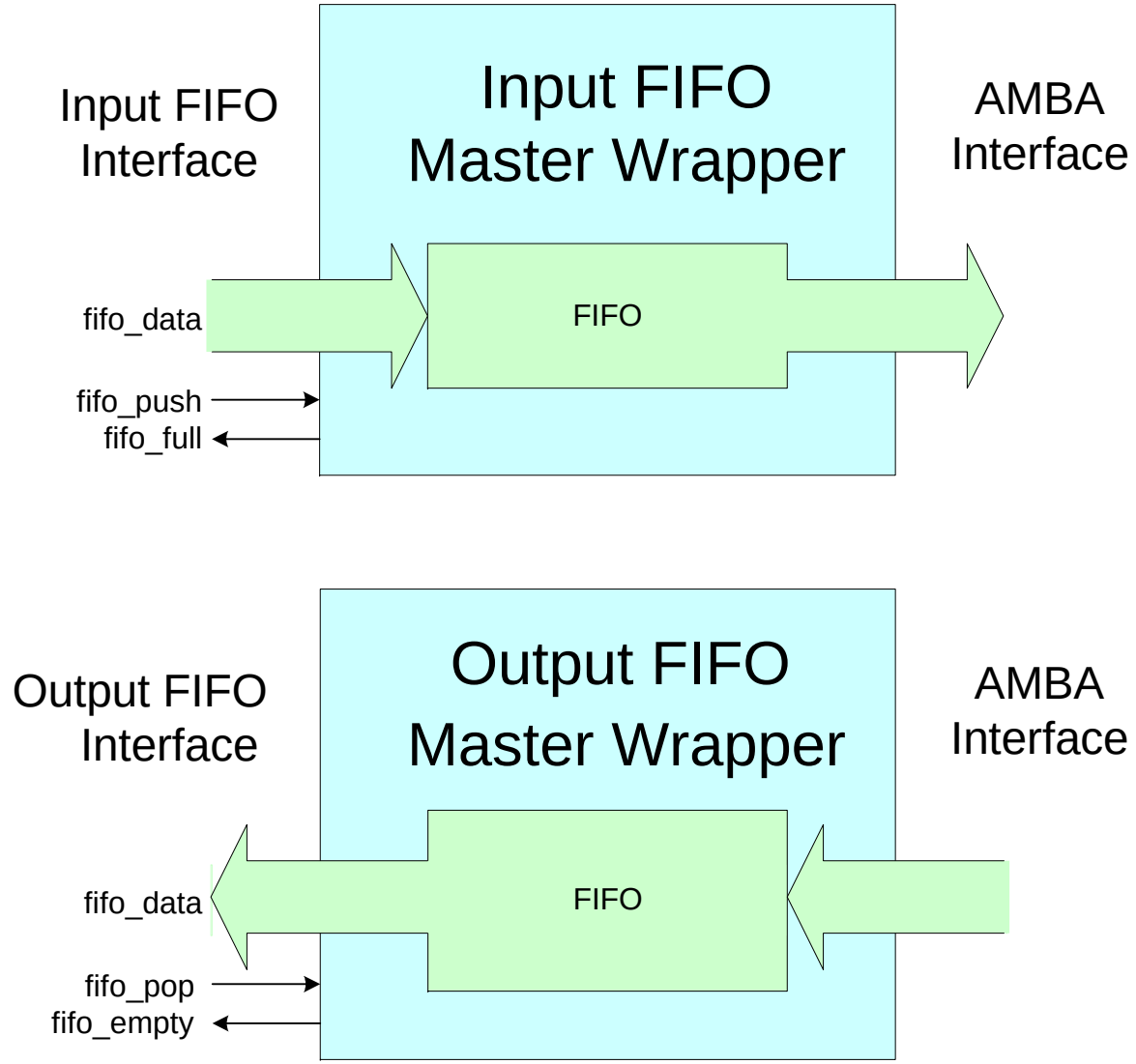
- Wrapper design guide
  - Separate core function and interface design

Processor Interface Wrapper

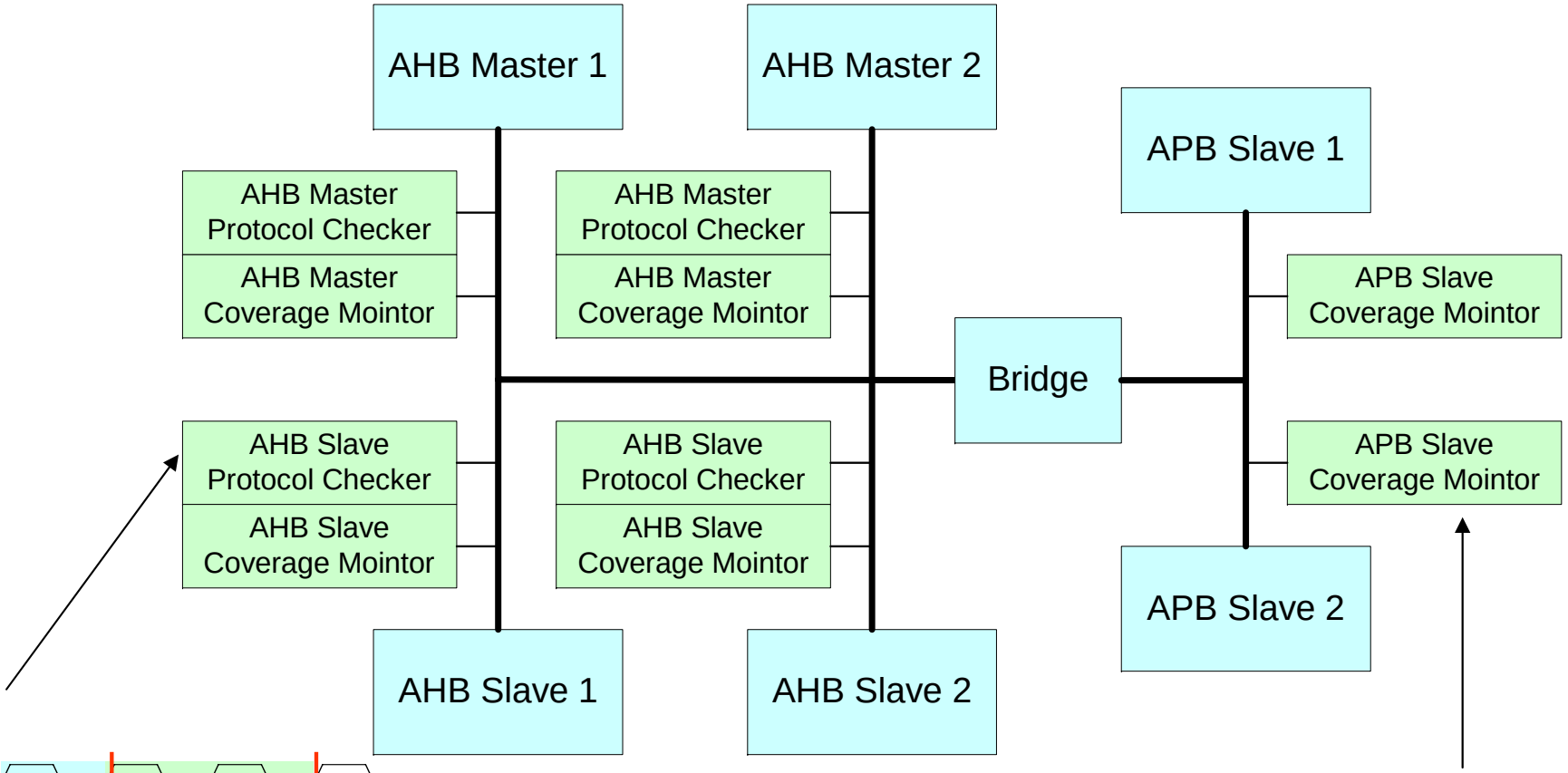


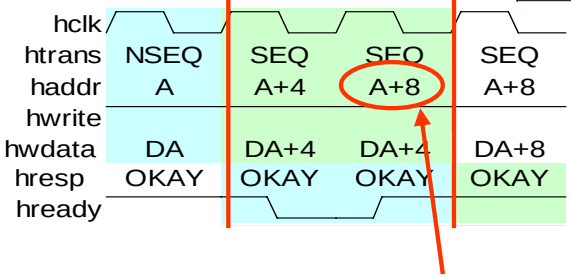
- DMA data channel transfer large block of data
- Data communication channel transfer single word data efficiently

FIFO Interface Wrapper



Verify AMBA System





AHB Master Protocol violation:
Address was changed while in transfer extension (hready low).
Ref. Spec. section 3.4

Transfer Response Summary

Response Type	Count
OKAY	104
ERROR	0
RETRY	5
SPLIT	13

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- Communication in a system
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- OCB's issues
- ***Conclusion***

Conclusion

- From buses to network
  - Get rid of idiosyncrasies such as buses and just move data from one point to another
  - Cost reduced due to the decreasing cost per gate
- Bus Protocols limits design of IP
  - Capture all of a core's communication requirements
  - Parameterizable Interface to tailor function and cost
- Chip-level test
  - Monitoring: from processor's task to hardware monitor