IP Core Design
Homework 4
Soft IP
for
Baseline JPEG Software Encoder

Instructor: Prof. Chein-Wei Jen
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In this homework, represent the C model(s) of your IP in homework 3 in synthesizable HDL. Make sure that your IP is AMBA-compliant and works correctly within both your own hardware testbench (HDL simulation environment) and ARM Integrator.

To make your IP more reusable, one should follow the *HDL coding guidelines*[1] and *FPGA Reuse Field Guide*[2]. Also, providing both complete deliverables [3] and self-measurement for IP reusability [4] is recommended; otherwise one-page description of your IP (e.g., [5]) and a datasheet (e.g., a condensed version of [6]) have to be provided. These documents can be written in Chinese or English.

[1] Michael Keating and Pierre Bricaud, "Reuse Methodology Manual for System-on-A-Chip Designs," 2ed. 1999.
[2] FPGA Reuse Field Guide, by Qualis Design Corporation Revision 03_2000_r1, 2000.
[3] Soft IP deliverables in IP contest 2001, http://vlsi.ee.ccu.edu.tw/~ip/Specification.htm
[4] OpenMORE Assessment Program, http://www.openmore.com/
[5] Baseline Motion-JPEG Encoder, Amphion , http://www.amphion.com/cs6100.html
[6] Motion JPEG VHDL Encoder/Decoder Core, Rev. 1.2, Nov 2000, 4i2i Communications Ltd, http://www.4i2i.com/M-JPEG_V12.PDF

Deliverable

Your deliverable has to include:

1. Report that describes your idea and result.
2. Documents like [3] ~ [6]
3. Source code of your JPEG encoder, hardware models, and drivers.
4. All setting and information required for regenerating the result shown in your report, including scripts and settings for EDA tools.

Design and model those portions of JPEG baseline encoder that you want to improve the coding process through hardware accelerators. All the details of the registers, memory addresses of these registers, bit definitions, and drivers (initialization and interrupt behavior) of your IP(s) should be included in the IP datasheet. In addition to the description of the functionality of the IPs, the programmer's model (e.g., Section 4.6 of Integrator/AP User Guide), the behavior of the driver (initialization and interrupt behavior), and the coordination of hardware and software. The report should point out:

- *The mechanism to transfer intermediate data between host controller and your IP*
- *Verification strategy and design for testability strategy*
- *Identify the differences between the C models and HDL design of your IP, including the reasons of these differences.*
- *Cost of the hole IP, including hardware silicon cost, software driver and memory requirement (software code + hardware buffer)*

State your approaches, key ideas and results clearly and formally, and avoid redundant description. Your report can be written in Chinese or English. However, make sure your report is readable. A manual report won't degrade your score, unless it is scrabbled.

Important Date

Due : 5:00 p.m. Dec. 24, 2001

For more information

- The contents of this document: Kun-Bin Lee
- ARM development tools: contact the TA with the number = your team number %5

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