IP CORE Design

矽智產設計

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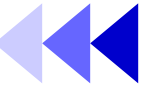
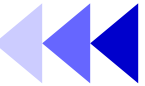
Course Contents



- Introduction to SoC and IP
- ARM processor core and instruction sets
- VCI interface, on-chip bus, and platform-based design
- IP core design flow, modeling and verification
- Algorithm and architecture exploration
- Some design studies

Reference Books



- Reuse Methodology Manual

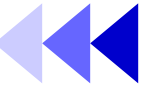
  for System-on-A-Chip Designs,

  By Michael Keating and Pierre Bricaud, 2ed. 1999
- ARM System-on-Chip Architecture

  By Steve Furber, 2ed. 2000
- VLSI Digital Signal Processing Systems

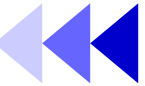
  By K.K. Parhi, 1999
- VSIA web site, www.vsi.org

Chapter 1



Introduction to System-on Chip and IP

SoC: System on Chip

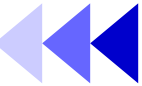


- System

  A collection of all kinds of components and/or subsystems that are appropriately interconnected to perform the specified functions for end users.

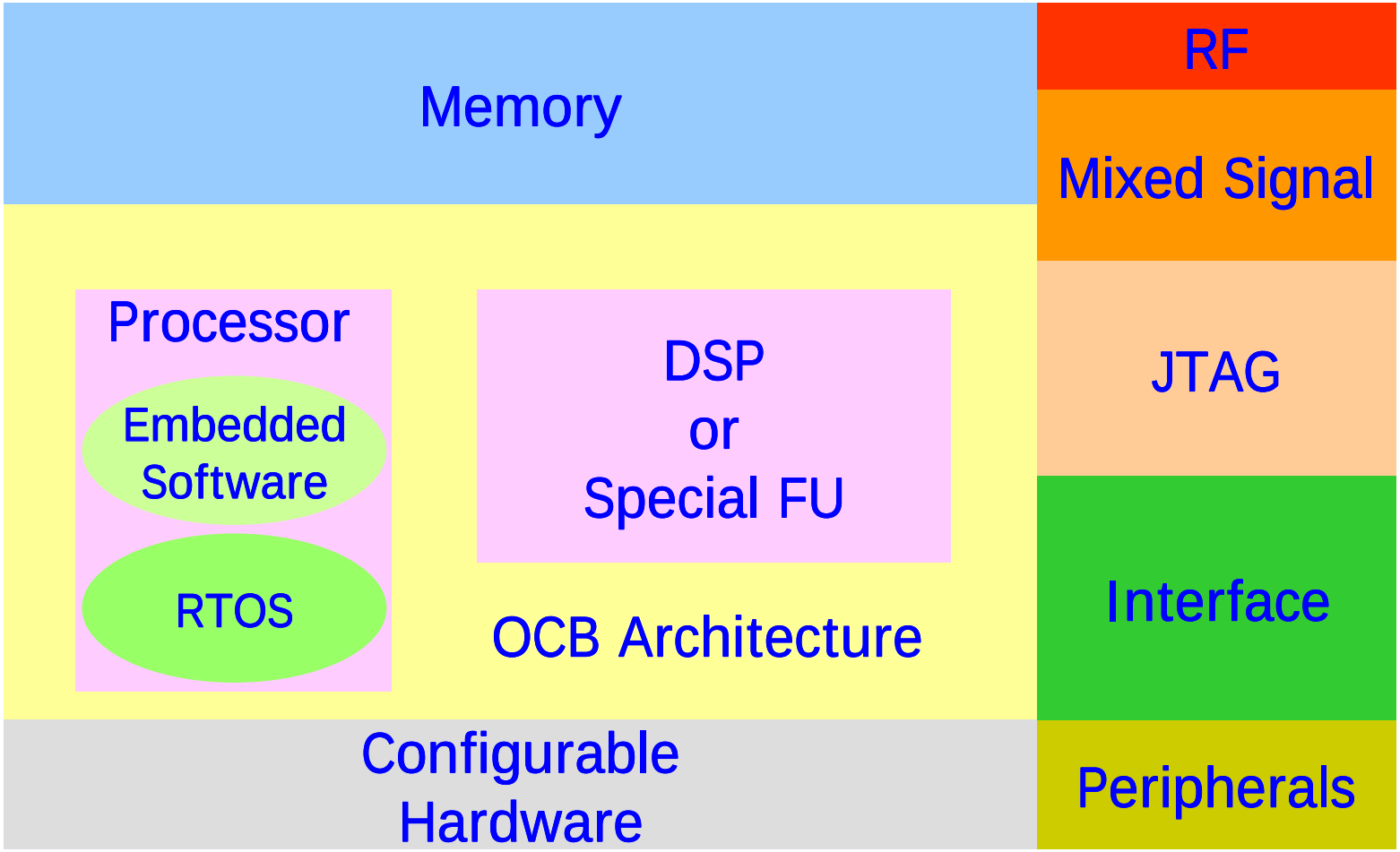
- A SoC design is a “product creation process” which
  - Starts at identifying the end-user needs
  - Ends at delivering a product with enough functional satisfaction to overcome the payment from the end-user

SoC

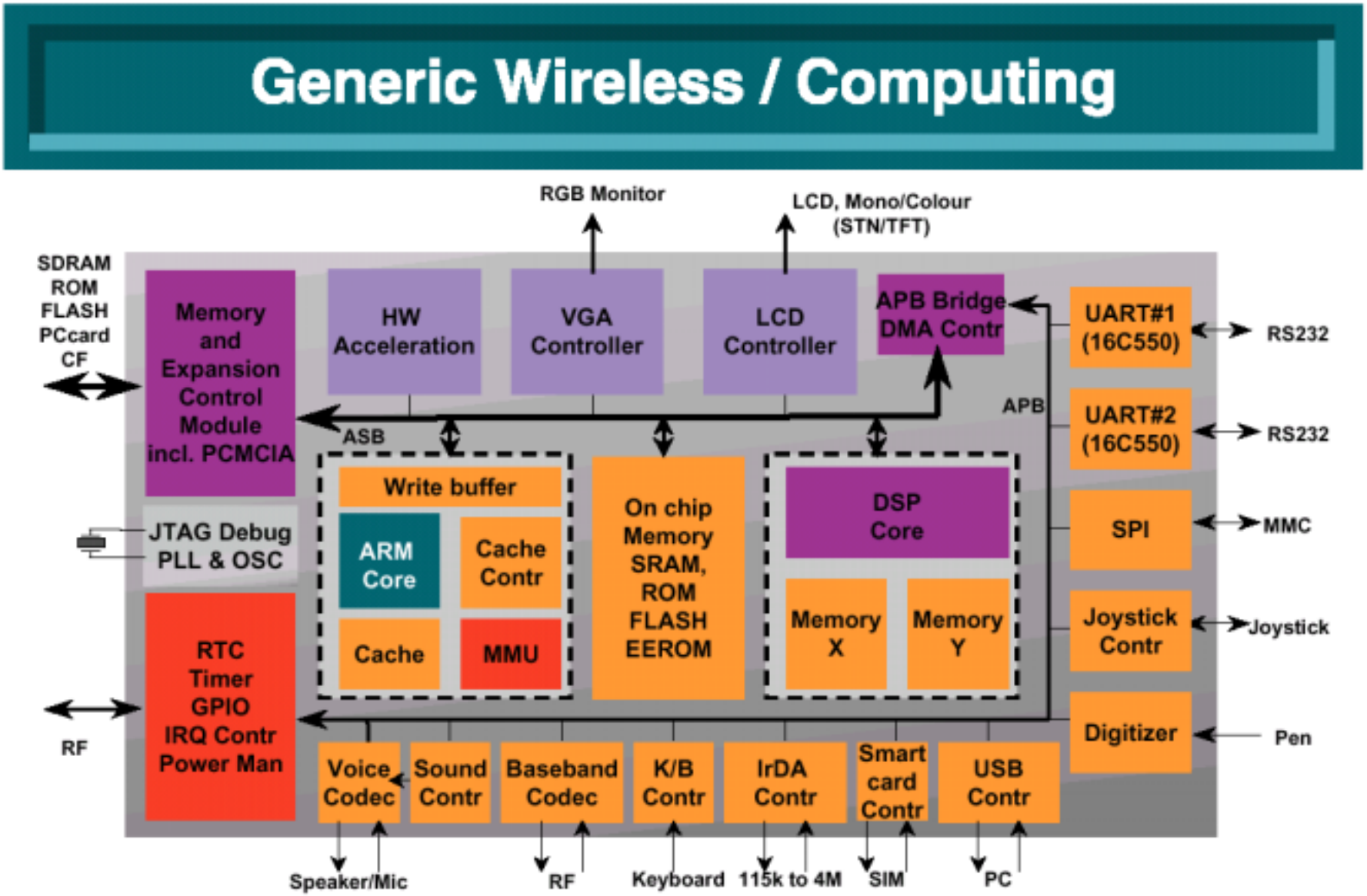


- Also named System-on-a-Chip. System LSI, System-on-Silicon, System-on-….
- It used to be System-on-a-board, or System-in-a-cabinet, or System-in-a-room
- System
  - Hardware
    - *Analog : ADC, DAC, PLL, TxRx, RF
    - *Digital : Processor, Interface, Accelerator
    - *Storage : SRAM, DRAM, FLASH, ROM
  - Software : OS, Application

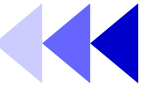
SoC Architecture



SoC - An Example

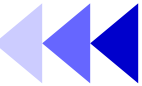


SoC Applications



- Communication
  - Digital cellular phone
  - Networking
- Computer
  - PC/Workstation
  - Chipsets
- Consumer
  - Set top box
  - Game box
  - Digital camera

Benefits of Using SoC



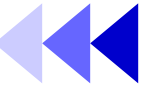
- Reduce overall system cost
- Increase performance
- Lower power consumption
- Reduce size

Evolution of Silicon Design

Year	1997	1998	1999	2002
Process Technology	0.35u	0.25u	0.18u	0.13u
Design Cycle (month)	18 ~ 12	12 ~ 10	10 ~ 8	8 ~ 6
Derivative Cycle (month)	8 ~ 6	6 ~ 4	4 ~ 2	3 ~ 2
Silicon Complexity (gate)	200 ~ 500 k	1 ~ 2 M	4 ~ 6 M	10 ~ 25 M
Applications	Cellular, PDAs, DVD	Set-top boxes, Wireless PDA	Internet appliances, Anything portable	Ubiquitous computing Intelligent, inter-connected con-trollers

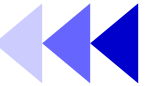
Source: "Surviving the SOC Revolution - A Guide to Platform-Based Design" by Henry Chang et al, Kluwer Academic Publishers, 1999

Challenges in SoC Era



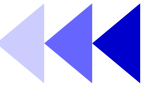
- Time-to-market
  - Process roadmap acceleration
  - Consumerization of electronic devices
- Complex systems
  - μCs, DSPs, HW/SW, SW protocol stacks, RTOS's, digital/analog IPs, On-chips buses
- Deep submicron effects
  - Crosstalk, electronmigration, wire delays, mask costs

How to Conquer the Complexity



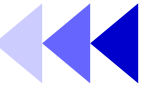
- Use a known real entity
  - A pre-designed component (IP reuse)
  - A platform (architecture reuse)
- Partition
  - Based on functionality
  - Hardware and software
- Modeling
  - At different level
  - Consistent and accurate

What is IP?



- Intellectual Property (IP)
  - Intellectual Property means products, technology, software, etc. that have been protected through patents, copyrights, or trade secrets.
- Virtual Component (VC)
  - A block that meets the Virtual Socket Interface Specification and is used as a component in the Virtual Socket design environment. Virtual Components can be of three forms — Soft, Firm, or Hard. (VSIA)
- Also named mega function, macro block, reusable component

Reusable Component

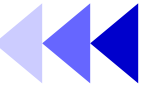


- A design object
  This refers to the type of components for which a physical implementation exists that can be reused. For example, ALU chips or macrocells that can be embedded in larger chips, etc. These designs are largely implemented in specific technologies. Limited parameterization may be possible. These design objects typically exist in technology libraries from one or more suppliers.
  ---- EDA Industry Standard Roadmap 1996

Types of IP

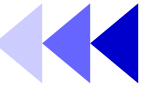
	Design Flow	Representation	Libraries	Technology	Portability
Soft - Very flexible - Not predicable	System Design RTL Design	Behavioral RTL	N/A	Technology Independent	Unlimited
Firm - Flexible - Predicable	Synthesis Floorplanning Placement	RTL & Constraints Netlist	Reference Library - Footprint - Timing model - Wiring model	Technology Generic	Library Mapping
Hard - Not flexible - Very predicable	Routing Verification	Polygon Data	Specific Library - Characterized cells - Fixed process rules	Technology Fixed	Process Porting

IP Value



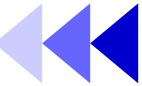
- Foundation IP – Cell, MegaCell
- Star IP – ARM (low power)
- Niche IP – JPEG, MPEGII, TV, Filter
- Standard IP – USB, IEEE1394, ADC, DAC
- ……..

IP Sources



- Legacy IP
  - from previous IC
- New IP
  - specifically designed for reuse
- Licensed IP
  - from IP vendors

Why IP

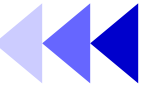


- Don’t know how to do it
- Cannot wait for new in-house development
- Standard/Compatibility calls for it
  - PCI, USB, IEEE1394, Bluetooth
  - software compatibility

Differences in Design Between IC and IP

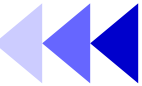
- Limitation of IC design
  - Number of I/O pin
  - Design and Implement all the functionality in the silicon
- Soft IP
  - No limitation on number of I/O pin
  - Parameterized IP Design: design all the functionality in HDL code but implement desired parts in the silicon
  - IP compiler/Generator: select what you want !!
  - More high level auxiliary tools to verify design
  - More difficult in chip-level verification
- Hard IP
  - No limitation on number of I/O pin
  - Provide multiple level abstract model
  - Design and Implement all the functionality in the layout

SIP Contest (1999)



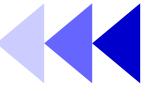
- Memory Interface Socket
- Blowfish Cipher
- 高階三角積分調變器之合成軟體
- 32-bit Embedded Microprocessor
- JPEG Encoder IP Design
- New Synthesizable Digital Frequency Synthesizer

SIP Contest (2000)



- Reusable Embedded in-Circuie Emulator
- High-speed Serial Bus IEEE 1394 Link and Digital PHY IP
- MAC IP and its Design Environment
- Multiply-And-Accumulator Unit Generator
- 32-bit Embedded Microprocessor and its Verification Environment
- A Programmable Arbiter for SoC Application

SIP Contest (2001)



- A Parameterized HDL Generator for Reed-Solomon Decoder
- Design of A RAM-based Internet Protocol Routing Table Lookup
- Design and Verification of An ARM9-like Embedded Microprocessor
- A Novel Architecture for Arithmetic Coding
- A Rijndael Cipher Chip for Advanced Encryption Standard