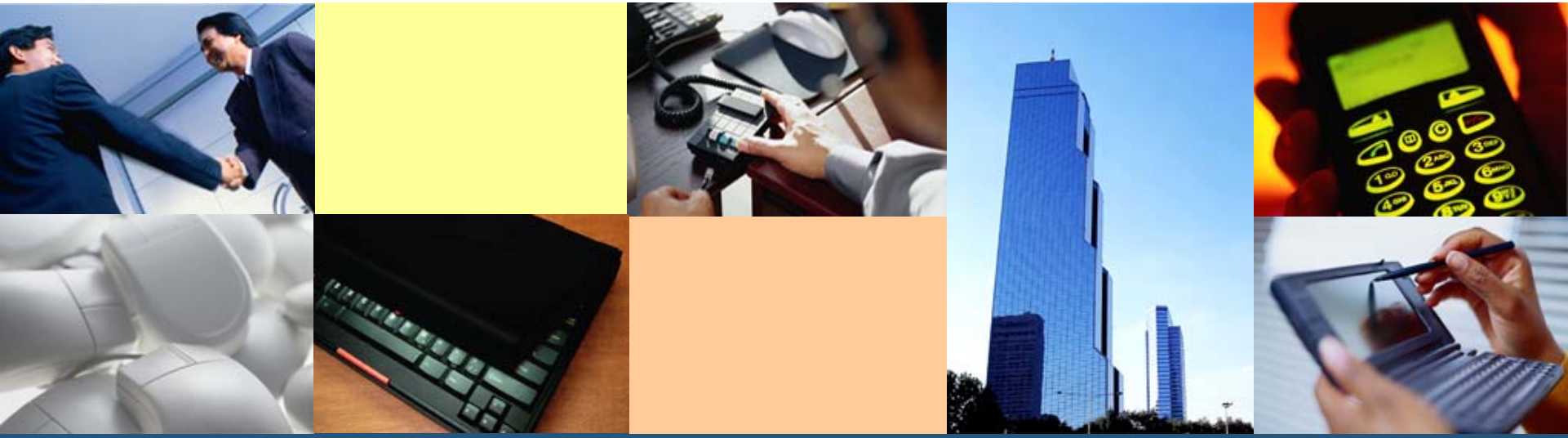
ANDES TECHNOLOGY

國立交通大學 National Chiao Tung University

AndesCore N1213-S



AndesCore™ N1213-S

CPU Core

- 32bit CPU
- Single issue with 8-stage pipeline
- AndeStar™ ISA with 16-/32-bit intermixable instructions to reduce code size
- Dynamic branch prediction to reduce branch penalties
  - 32/64/128/256 BTB

Configurability for customers

- Configuration options for power, performance and area requirements

AndesCore™ N1213-S

❖ MMU

- fully-associative iTLB/dTLB: 4 or 8 entries
- 4-way set-associative main TLB: 32/64/128 entries
- Two groups of pages size support: (4K,1M) and (8K,1M)
- Locking support for TLB

❖ I & D cache

- Virtual index and physical tag (for faster context switching)
- Cache size: 8KB/16KB/32KB/64KB
- Cache line size: 16B/32B
- 2/4-way set associative
- I Cache locking support

AndesCore™ N1213-S

- **I & D Local memory**
  - wide range support for internal /external local memory
    - 4KB~1024KB
  - Provide fixed access latencies for internal local memory
  - Double buffer mode for D local memory
  - Optional external local memory interface
- **Bus**
  - Synchronous/Asynchronous AHB
    - 1 or 2 port configuration
  - Synchronous HSMP
    - AXI like
    - 1 or 2 port configuration

AndesCore™ N1213-S

For performance

- Improved memory accesses:
  - 1D/2D DMA, load/store multiple
- Efficient synchronization without locking the whole bus
  - Load lock, store conditional instructions
- Vectored interrupt to improve real-time performance
  - 6 interrupt signals
- MMU
  - Optional HW page table walker
  - TLB management instructions

For flexibility

- Memory-mapped IO space
- PC-relative jumps for position independent code
- JTAG-based debug support
- Optional embedded program trace interface
- Performance monitors for performance tuning
- Bi-endian modes to support flexible data input

AndesCore™ N1213-S Overview

- **For power Management**
  - Clock-gated pipeline
  - Low-power mode support instructions
  - Redundant memory access reduction
  - Many CPU/bus frequency ratio support

Cache SRAM example – 32KB

- Instruction cache tag
  - 256 (cache line#) x 4 (ways) x 22
  - 22={Valid (1), Lock (1), index (20)}
- Instruction cache data (32KB)
  - 2048 (entry #) x 32bit x 4 (ways)
- Data cache tag
  - 256 (cache line#) x 4 (ways) x 22
- Data cache data (32KB and byte access)
  - 2048 (entry #) x 8x4bit x 4 (ways)

N1213-S Cache configuration

- **Cache sets per way**
  - 128/256/512
- **Cache ways**
  - 2/4 ways
- **Cache line size**
  - 16B/32B
- **Cache size combination**
  - 256X16BX2=8KB
  - 128X32BX2=8KB
  - 256X16BX4=16KB
  - 512X16BX2=16KB
  - 128X32BX4=16KB
  - 256X32BX2=16KB
  - 256X32BX4=32KB
  - 512X32BX2=32KB
  - 512X16BX4=32KB
  - 1024X16BX2=32KB
  - 512X32BX4=64KB
  - 1024X16BX4=64KB

Cache replacement algorithm

- Pseudo LRU (default)
- Random

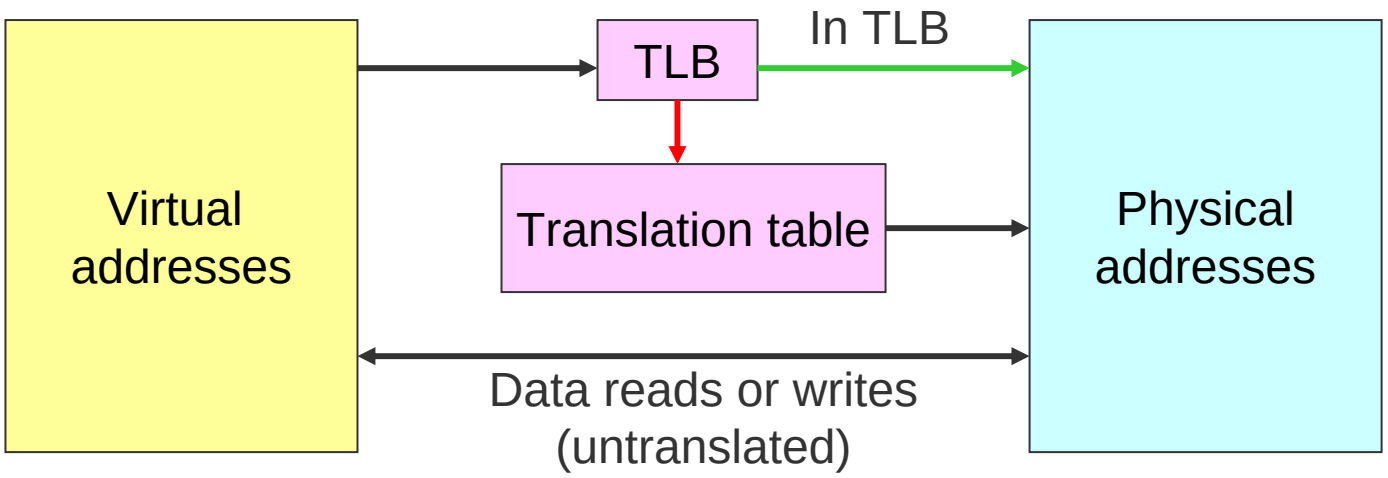
MTLB entry:63bit

- **MTLB tag**
  - VPN[31:12]: Virtual page number
    - 4KB : VPN[31:12]
    - 8KB : VPN[31:13]
  - CID[8:0]:process ID
  - G :Global bit
  - S :S=1 1MB page table
  - Valid
  - Lock
- **MTLB data**
  - D : dirty bit
  - X : executable bit
  - A : accessed bit
  - PPN[31:12]: Physical page number
  - C[2:0] : Cacheability attributes
  - M[2:0] :Access privilege for user and superuser mode
- **MTLB configuration options**
  - 32x4=128
  - 16x4=64
  - 8x4=32

Caching Applied to Address Translation

- Process references the same page repeatedly
  - Translating each virtual address to physical address is wasteful
- Translation lookaside buffer (TLB)
  - Track frequently used translations
  - Avoid translations in the common case

Caching Applied to Address Translation



Example of the TLB Content

Virtual page number (VPN)	Physical page number (PPN)	Control bits
2	1	Valid, rw
-	-	Invalid
0	4	Valid, rw

TLB Lookups

- Sequential search of the TLB table
- Direct mapping: assigns each virtual page to a specific slot in the TLB
  - e.g., use upper bits of VPN to index TLB

Direct Mapping

```
if (TLB[UpperBits(vpn)].vpn == vpn) {
  return TLB[UpperBits(vpn)].ppn;
} else {
  ppn = PageTable[vpn];
  TLB[UpperBits(vpn)].control = INVALID;
  TLB[UpperBits(vpn)].vpn = vpn;
  TLB[UpperBits(vpn)].ppn = ppn;
  TLB[UpperBits(vpn)].control = VALID |
  RW
  return ppn;
}
```

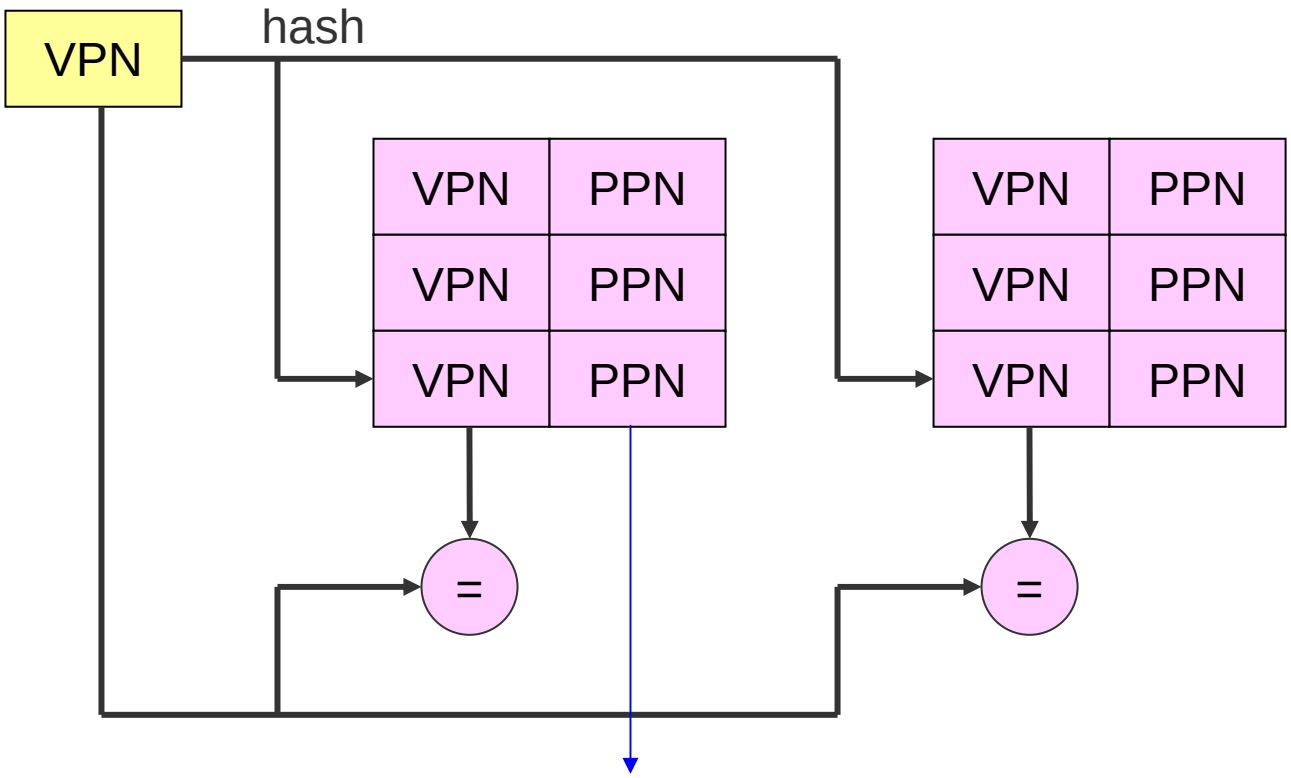
Direct Mapping

- When use only high order bits
  - Two pages may compete for the same TLB entry
    - May loss out needed TLB entries
- When use only low order bits
  - TLB reference will be clustered
    - Failing to use full range of TLB entries
- Common approach: combine both

TLB Lookups

- Set associatively: use N TLB banks to perform lookups in parallel

Two-Way Associative Cache

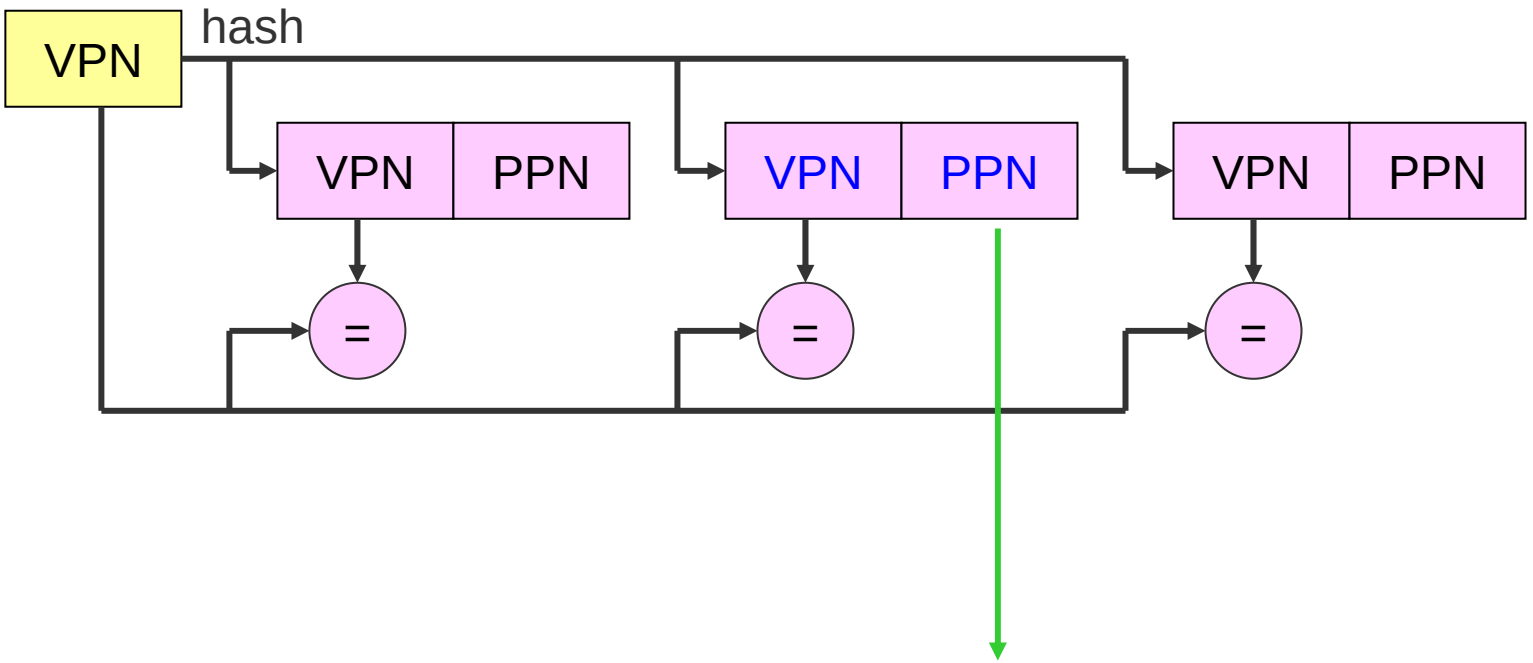


If miss, translate and replace one of the entries

TLB Lookups

- Fully associative cache: allows looking up all TLB entries in parallel

Fully Associative Cache



If miss, translate and replace one of the entries

TLB Lookups

- Typically
  - TLBs are small and fully associative
  - Hardware caches use direct mapped or set-associative cache

Replacement of TLB Entries

- Direct mapping
  - Entry replaced whenever a VPN mismatches
- Associative caches
  - Random replacement
  - LRU (least recently used)
  - MRU (most recently used)
  - Depending on reference patterns

Replacement of TLB Entries

- Hardware-level
  - TLB replacement is mostly random
    - Simple and fast
- Software-level
  - Memory page replacements are more sophisticated
  - CPU cycles vs. cache hit rate

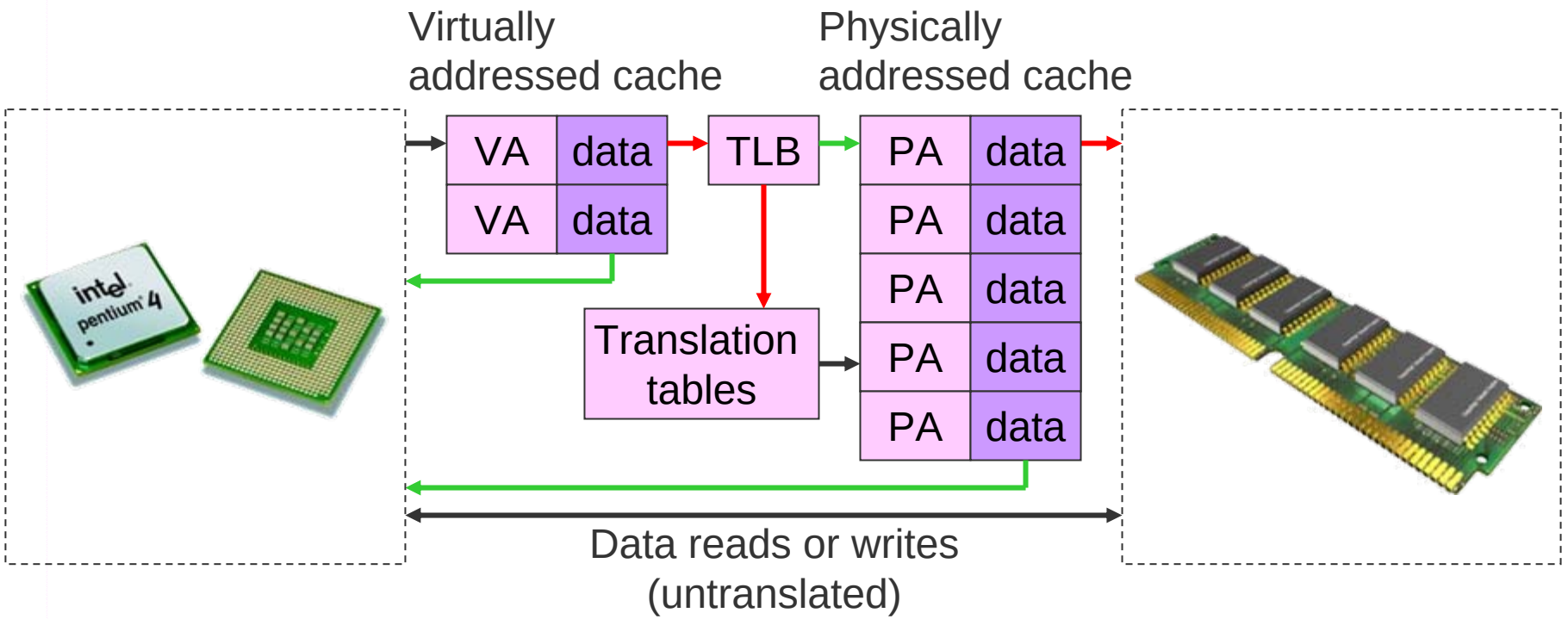
Consistency Between TLB and Page Tables

- Different processes have different page tables
  - TLB entries need to be invalidated on context switches
  - Alternatives:
    - Tag TLB entries with process IDs
    - Additional cost of hardware and comparisons per lookup

Relationship Between TLB and HW Memory Caches

- We can extend the principle of TLB
- Virtually addressed cache: between the CPU and the translation tables
- Physically addressed cache: between the translation tables and the main memory

Relationship Between TLB and HW Memory Caches



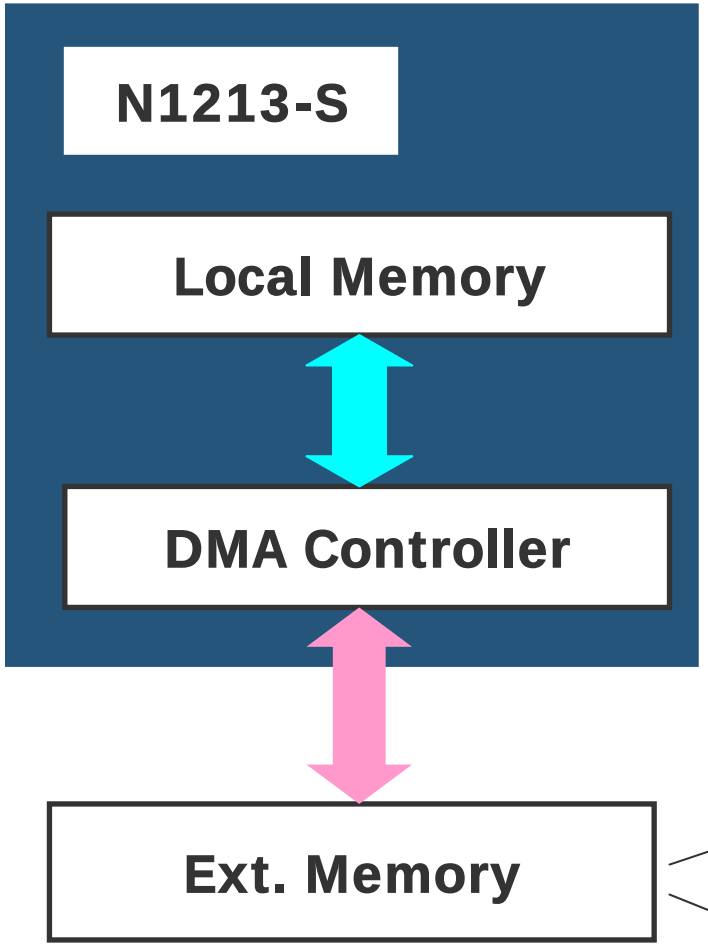
Support Inter./ext. vector interrupt

- Internal vector interrupt
  - where interrupts are prioritized inside an AndesCore™
  - Hw0 has highest priority
- External Vectored Interrupt
  - where interrupts are prioritized outside AndesCore using an external interrupt controller.
- The size of the vectored entry point can be from 4 bytes to 16/64/256 bytes.

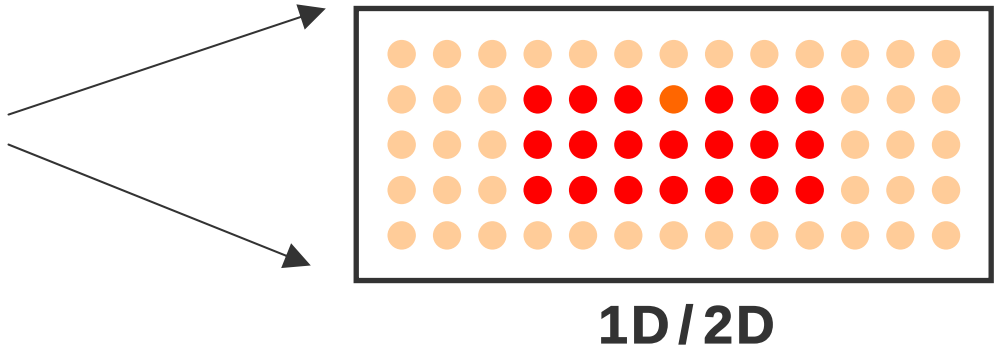
Local memory

- Internal or external local memory configuration options
- Two different access modes for internal local memory
  - Normal access mode
  - Double buffer mode
    - 2 bank structure
    - ½ local memory size
    - CPU and DMA can access the same time

DMA



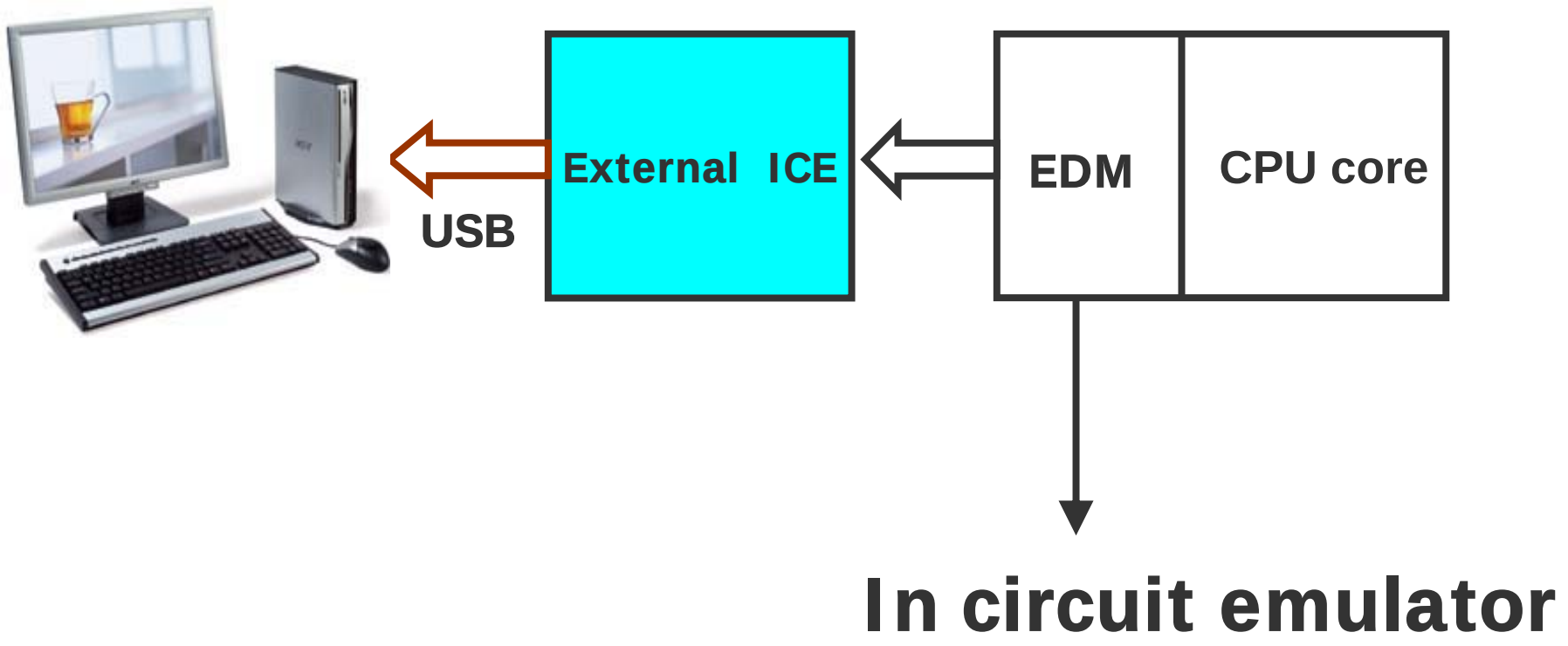
- Two channels
- One active channel
- Only accessed by superuser mode
- For both instruction and data local memory
- External address can be incremented with stride
- Optional 2-D Element Transfer from external memory



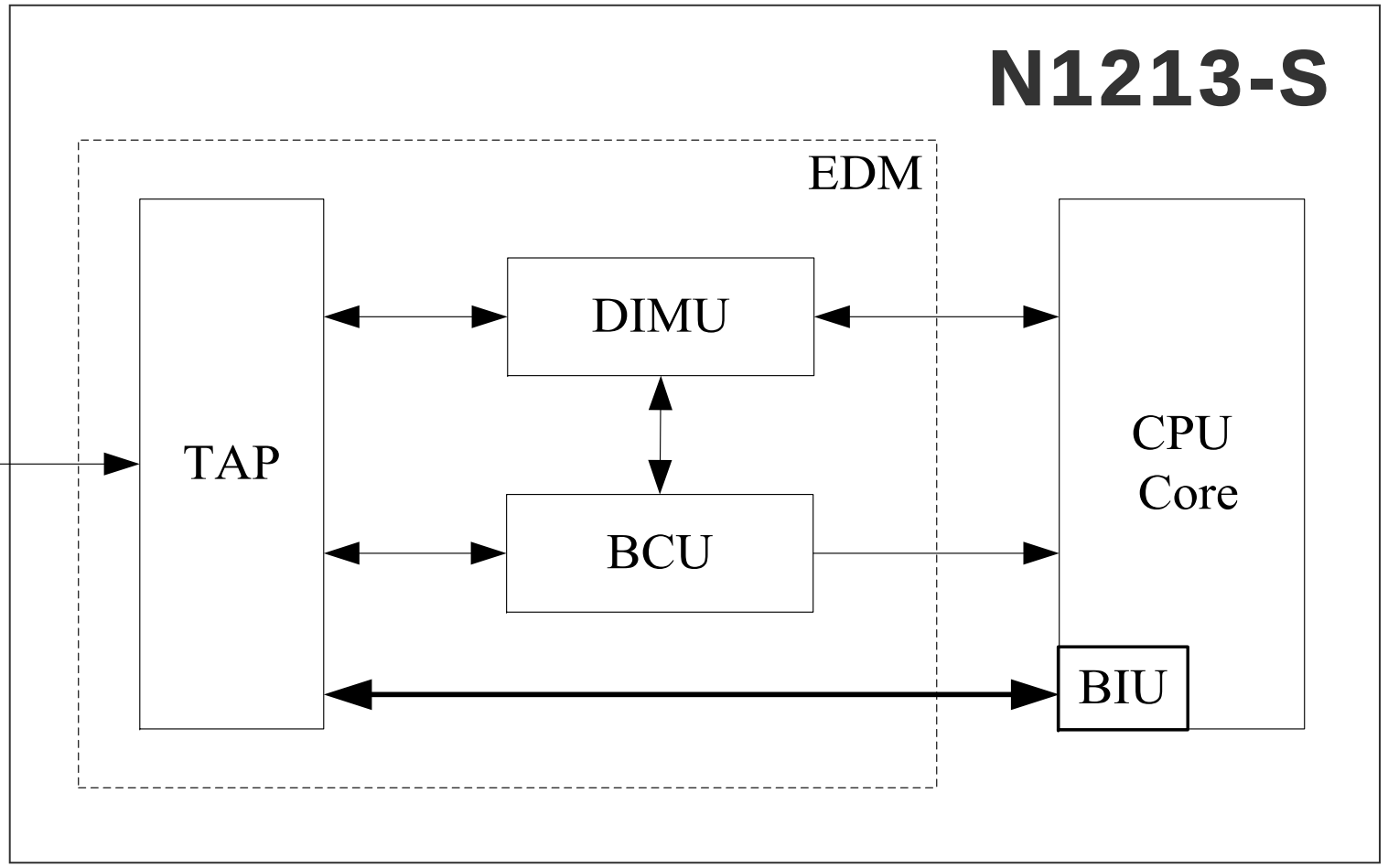
N1213-S BUS

- AMBA 2.0 AHB bus
  - 1 port
  - 2 port
    - ICU/MMU (read only) for port 1
    - LSU/DMA/EDM (read/write) for port 2
- HSMP
  - High speed memory port
  - Same frequency with CPU core
  - AMBA 3.0 (AXI) protocol compliant, but with reduced I/O requirements
  - 1 and 2 port configuration

N1213-S Debug environment



EDM (Embedded Debug Module) block diagram



TAP:JTAG style interface

DIMU: Store debug program

BCU: Breakpoint compare unit

Performance Monitor

Performance Counter 0

Performance Counter 1

Performance Counter 2

CPU Clock Cycle

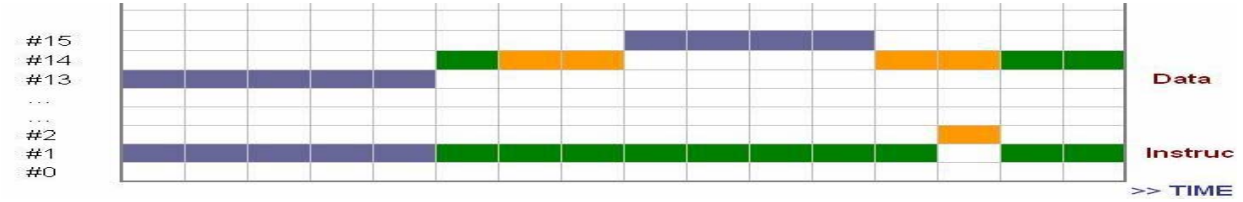
CPU Cycle Counting

CPU Instruction Executions …

Instruction Counting

Memory and Cache Access

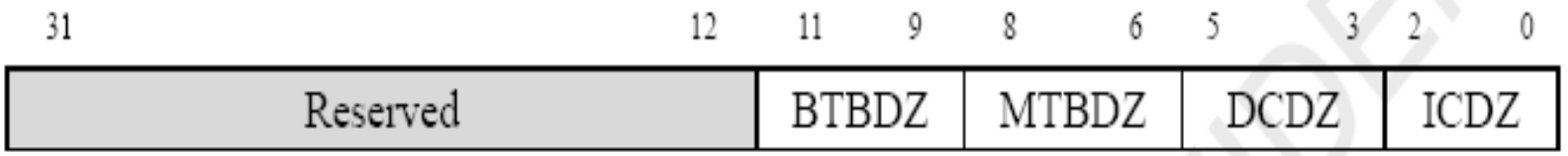
Cache Miss Event



Branch or Other Events …

Downsizing control

Structure Downsizing Control Register



This control register allows customers to emulate smaller cache structures on Andes hardcore. This control feature is intended to help customers to figure out the best cache configurations for their final products.

Field Name	Bits	Description	Type	Reset
ICDZ	3 (2,0)	Instruction Cache downsizing control. Value / Meaning: 0 – maximum size with 4-way-set 1 – maximum size/2 with 2-way-set 2 – maximum size/2 with 4-way-set 3 – maximum size/4 with 2-way-set 4-7 – Unassigned/UNPREDICTABLE	RW	0

Downsizing control

		1 maximum size/2 with 2-way-set 2 maximum size/2 with 4-way-set 3 maximum size/4 with 2-way-set 4-7 Unassigned/UNPREDICTABLE		
MTBDZ	3 (8,6)	MTLB downsizing control. Value: 0 maximum size with 4-way-set; 1 maximum size/2 with 2-way-set; 2 maximum size/2 with 4-way-set; 3 maximum size/4 with 2-way-set; 4-7 Unassigned/UNPREDICTABLE	RW	0
BTBDZ	3 (11,9)	Branch Target Table downsizing control. Value: 0 maximum size with 2-way-set; 1 maximum size/2 with direct-map; 2 maximum size/2 with 2-way-set; 3 maximum size/4 with direct-map; 4-7 Unassigned/UNPREDICTABLE	RW	0
Reserved	20 (31,12)	RAZWI	-	0

32KB

16KB

128-entry

64-entry

64X2(Max size=128)

32X2

64

32X1

- Cache and MTLB for 4 way only

Signal pins

- General port signals
  - Reset, CPU clock, AHB clock, Bus_CLOCK_Phase
- Configuration port signals
  - Endian setting
  - IVB (initial vector base)
- Interrupt port signals
- AHB interface signal
- Multi-core lock signal
- HSMP interface signal
- Power management
  - Standby, Wakeup
- EDM interface signals
- Tracer interface signals
- Test port signals
  - Scan, Mbist, …..
- Optional external local memory interface signals

Clock ratio

- The clock bus ratio between CPU core and AMBA bus clock are 1/1,2/1,3/1,4/1,5/1,6/1,3/2,5/2,8/1,10/1,12/1,14/1, 15/1,18/1,20/1.
  - Clock divider is not part of AndesCore
- While the high speed memory bus clock is the same with CPU core clock.

Configuration options

- Cache size (I & D)
  - 256X16BX2=8KB
  - 128X32BX2=8KB
  - 256X16BX4=16KB
  - 512X16BX2=16KB
  - 128X32BX4=16KB
  - 256X32BX2=16KB
  - 256X32BX4=32KB
  - 512X32BX2=32KB
  - 512X16BX4=32KB
  - 1024X16BX2=32KB
  - 512X32BX4=64KB
  - 1024X16BX4=64KB
  - Direct map 2 or 4 bank
  - Write through only (D cache)
- Cache policy
  - Pseudo-LRU (default), Random

Configuration options

- Instruction queue
  - 2/4/8
- u-ITLB-entry/ u-DTLB-entry
  - 4 or 8
- MTLB-entry
  - 8x4 (way)=32
  - 16x4=64
  - 32x4=128
- BTB-entry
  - 16x2 (way)=32
  - 32x2 =64
  - 64x2=128
  - 128X2=256
- Internal or external local memory
- ILM/DLM
  - 4KB/8KB/16KB/32KB/64KB/128KB/256KB/512KB/1024KB

Configuration options

- AHB port
  - 1 or 2
- HSMP
  - 1 or 2
- AHB clock synchronization
  - Synchronous (default) or Asynchronous
- EDM break point
  - 0/1/2/3/4/5/6/7/8

Configuration options

- Optional (exist or not)
  - HPTW (hardware page table walker)
  - 16bit ISA
  - Performance extension ISA
  - MAC related ISA (refer to MSC_CFG)
  - ICE
  - EPT interface
  - Performance monitor
  - Gated clock

Configuration Options (1)

Andes N1213-S Softcore Configure - Deer Park

File Edit View Go Bookmarks Tools Help

file:///home/users/arthur_w/projects/work1/pvc_whitiger/tools/src/Configure/www/com.andestech.Configure/Configure.html

Red Hat Network Support Shop Products Training

Generate config.inc | Generate settings for syn_env.tcl | Generate ISS options

▽ Branch Target Buffer	
Size (entries)	○ 32 ○ 64 ◉ 128 ○ 256
Associativity	◉ 2-way (non-configurable)
Instruction Queue Size	
Size (entries)	◉ 2 ○ 4 ○ 8
Cache Line Size	
Size (bytes)	○ 16B ◉ 32B
▽ Instruction Cache	
Size (KB)	○ 8KB ○ 16KB ◉ 32KB ○ 64KB
Associativity	○ direct-map ○ 2-way ◉ 4-way
Banks (direct-map only)	◉ 2 banks ○ 4 banks
Replacement Policy	◉ pseudo LRU ○ random
▽ Data Cache	
Size (entries)	○ 8KB ○ 16KB ◉ 32KB ○ 64KB
Associativity	○ direct-map ○ 2-way ◉ 4-way
Banks (direct-map only)	◉ 2 banks ○ 4 banks
Replacement Policy	◉ pseudo LRU ○ random
Writethrough Only	☐
☐ Software downsizing support (require 32KB/64KB 4way caches)	
▽ Instruction Local Memory	
Mode	◉ Internal ○ External
Size	○ 4KB ○ 8KB ◉ 16KB ○ 32KB ○ 64KB ○ 128KB ○ 256KB ○ 512KB ○ 1MB
▽ Data Local Memory	
Mode	◉ Internal ○ External
Size	○ 4KB ○ 8KB ◉ 16KB ○ 32KB ○ 64KB

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Configuration Options (2)

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file:///home/users/arthur_w/projects/work1/pvc_whitiger/tools/src/Configure/www/com.andestech.Configure/Configure.html

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Data Local Memory	
Mode	Internal / External
Size	4KB / 8KB / 16KB / 32KB / 64KB / 128KB / 256KB / 512KB / 1MB
DMA Support (require ILM and/or DLM)	
Memory Management Unit	
Instruction microTLB size	4 entries / 8 entries
Data microTLB size	4 entries / 8 entries
Main TLB size (4-way per set)	32 entries (8 sets) / 64 entries (16 sets) / 128 entries (32 sets)
Hardware Page Table Walker	☑
Bus Interfaces	
AMBA Bus	☑
Number of AHB Ports	1 port / 2 ports
AHB Clock Synchronization	Asynchronous / Synchronous
HSMP Bus	☐
Number of HSMP Ports	1 port / 2 ports
Embeded Debug Module	
Number of Breakpoints	1 / 2 / 3 / 4 / 5 / 6 / 7 / 8
Embeded Program Tracer Interface	☐
Instruction Set Options	
16-bit Instructions	☑
Performance Extension	☑
MAC	☑
Performance Monitor	
Gated Clock	

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EDA tools

- Synthesizer
  - Synopsys Design Compiler
- Simulator
  - Cadence Incisive
- Formal verification
  - Cadence Formality
- STA
  - Synopsys PrimeTime
- FPGA
  - Synplicity +Xilink

N1213 on UMC 0.13HS process

Items	Values
Product name	N1213_43U1H (Hardcore)
Fab/process	UMC/L130E-HS
Branch prediction entry number	128
I Cache size (Bytes)	32K
D Cache size (Bytes)	32K
Cache line size (Bytes)	32
Cache associative (way)	4
I Local memory (Bytes)	16K
D Local memory (Bytes)	16K
iTLB (fully associative) entry number	4
dTLB (fully associative) entry number	8
Main TLB (4-way set associative) entry number	128
Hardware page table walker	yes
DMA	yes
Max Clock Frequency (*Worst case) (Mhz)	500
Size (mm^2)	3.44x 2.31
Number of metal layers used	6

* 1.08V 125C slow silicon

Market position

CPU requirement	Applications	Target process (um)
High performance	Set top box	0.13, 0.09
	Digital home	
	DTV	
	DVDR	
	Switch /router	
	Gateway	
	MFP	
	Game console	
High performance, low power	Mobile phone	0.13, 0.09, 0.065
	Handheld game	

Thank You