LCDC	0x90600000 + 0x00	LCD Timing0	LCD horizontal timing control
LCDC	0x90600000 + 0x04	LCDTiming1	LCD vertical timing control
LCDC	0x90600000 + 0x08	LCDTiming2	LCD clock and signal polarity control

Module Name	Address	Name	Description
LCDC	0x90600000 + 0x10	LCDFrameBase	LCD panel frame base address
LCDC	0x90600000 + 0x18	LCDIntEnable	LCD interrupt enable mask
LCDC	0x90600000 + 0x1C	LCDControl	LCD panel pixel parameters
LCDC	0x90600000 + 0x20	LCDInClr	LCD interrupt clear
LCDC	0x90600000 + 0x24	LCDInterrupt	LCD masked interrupts
LCDC	0x90600000 + 0x34	OSDControl0	OSD scaling and dimension control
LCDC	0x90600000 + 0x38	OSDControl1	OSD position control
LCDC	0x90600000 + 0x3C	OSDControl2	OSD foreground color control
LCDC	0x90600000 + 0x40	OSDControl3	OSD background color control
LCDC	0x90600000 + 0x44	GPIOControl	GPI/GPO control
LCDC	0x90600000 + 0x200~ 0x90600000 + 0x3FC	PaletteWritePort	LCD palette RAM write access port
LCDC	0x90600000 + 8000~ 0x90600000 + 0xBFFC	OSDFontWritePort	OSD font database write access port
LCDC	0x90600000 + 0xC000~ 0x90600000 + 0xC7FC	OSDAttributeWritePort	OSD window attribute write access port

WDT	0x98500000 + 0x00	WdCounter	Watch Dog Timer Counter Register
WDT	0x98500000 + 0x04	WdLoad	Watch Dog Timer Counter Auto Reload Register
WDT	0x98500000 + 0x08	WdRestart	Watch Dog Timer Counter Restart Register
WDT	0x98500000 + 0x0C	WdCR	Watch Dog Timer Control Register
WDT	0x98500000 + 0x10	WdStatus	Watch Dog Timer Status
WDT	0x98500000 + 0x14	WdClear	Watch Dog Timer Clear
WDT	0x98500000 + 0x18	WdIntrCter	Watch Dog Timer Interrupt Length
RTC	0x98600000 + 0x00	RtcSecond	RTC Second Register
RTC	0x98600000 + 0x04	RtcMinute	RTC Minute Register
RTC	0x98600000 + 0x08	RtcHour	RTC Hour Register
RTC	0x98600000 + 0x0C	RtcDays	RTC Day Count Register
RTC	0x98600000 + 0x10	AlarmSecond	RTC Second Alarm Register
RTC	0x98600000 + 0x14	AlarmMinute	RTC Minute Alarm Register
RTC	0x98600000 + 0x18	AlarmHour	RTC Hour Alarm Register
RTC	0x98600000 + 0x1C	RtcRecord	RTC Record Register
RTC	0x98600000 + 0x20	RtcCR	RTC Control Register

GPIO	0x98700000 + 0x00	GpioDataOut	GPIO Data Output Register
GPIO	0x98700000 + 0x04	GpioDataIn	GPIO Data Input Register
GPIO	0x98700000 + 0x08	PinDir	GPIO Direction Register
GPIO	0x98700000 + 0x10	GpioDataSet	GPIO Data Bit Set Register
GPIO	0x98700000 + 0x14	GpioDataClear	GPIO Data Bit Clear Register
GPIO	0x98700000 + 0x18	PinPullEnable	GPIO Pull Up Register
GPIO	0x98700000 + 0x1C	PinPullType	GPIO Pull High Pull Low Register
GPIO	0x98700000 + 0x20	IntrEnable	GPIO Interrupt Enable Register
GPIO	0x98700000 + 0x24	IntrRawState	GPIO Interrupt Raw Status Register
GPIO	0x98700000 + 0x28	IntrMaskedState	GPIO Interrupt Masked Status Register
GPIO	0x98700000 + 0x2C	IntrMask	GPIO Interrupt Mask Register
GPIO	0x98700000 + 0x30	IntrClear	GPIO Interrupt Clear
GPIO	0x98700000 + 0x34	IntrTrigger	GPIO Interrupt Trigger Method Register
GPIO	0x98700000 + 0x38	IntrBoth	GPIO Interrupt Edge Trigger By Both
GPIO	0x98700000 + 0x3C	IntrRiseNeg	GPIO Interrupt Trigger by Rising or Falling Edge
GPIO	0x98700000 + 0x40	BounceEnable	GPIO Pre-scale Clock Enable. When enabled, PCLK will be divided by BouncePreScale clock.
GPIO	0x98700000 + 0x44	BouncePreScale	GPIO Pre-scale, which is used to adjust different

INTC	0x98800000 + 0x00	IRQSR	IRQ Source Register
INTC	0x98800000 + 0x04	IRQMR	IRQ Mask Register
INTC	0x98800000 + 0x08	IRQICR	IRQ Interrupt Clear Register
INTC	0x98800000 + 0x0C	IRQTMR	IRQ Trigger Mode Register
INTC	0x98800000 + 0x10	IRQTLR	IRQ Trigger Level Register
INTC	0x98800000 + 0x14	IRQSR	IRQ Status Register
INTC	0x98800000 + 0x20	FIQSR	FIQ Source Register
INTC	0x98800000 + 0x24	FIQMR	FIQ Mask Register
INTC	0x98800000 + 0x28	FIQICR	FIQ Interrupt Clear Register
INTC	0x98800000 + 0x2C	FIQTMR	FIQ Trigger Mode Register
INTC	0x98800000 + 0x30	FIQTLR	FIQ Trigger Level Register
INTC	0x98800000 + 0x34	FIQSR	FIQ Status Register
INTC	0x98800000 + 0x50	RRVISION	Revision Register
INTC	0x98800000 + 0x54	FRIN	Feature Register for Input Number
INTC	0x98800000 + 0x58	FRIDL	Feature Register for IRQ De-bounce Location
INTC	0x98800000 + 0x5C	FRFDL	Feature Register for FIQ De-bounce Location

I^2S/AC97	0x99400000 + 0x00	SSPCR0	SSP Control Register 0
I^2S/AC97	0x99400000 + 0x04	SSPCR1	SSP Control Register 1
I^2S/AC97	0x99400000 + 0x08	SSPCR2	SSP Control Register 2
I^2S/AC97	0x99400000 + 0x0C	SSPSR	SSP Status Register
I^2S/AC97	0x99400000 + 0x10	SSPICR	SSP Interrupt Control Register
I^2S/AC97	0x99400000 + 0x14	SSPISR	SSP Interrupt Status Register
I^2S/AC97	0x99400000 + 0x18	SSPDR	SSP Data Register
I^2S/AC97	0x99400000 + 0x20	SSPVR	AC-link Slot Valid Register