1.5

a.

performance of P1 (instructions/sec) = $3.0*10^9/1.5 = 2*10^9$
performance of P2 (instructions/sec) = $2.5*10^9/1.0 = 2.5*10^9$
performance of P3 (instructions/sec) = $4.0*10^9/2.2 = 1.8*10^9$

b.

cycles of P1 = $10*3.0*10^9 = 30*10^9$
cycles of P2 = $10*2.5*10^9 = 25*10^9$
cycles of P3 = $10*4.0*10^9 = 40*10^9$
No. instructions of P1 = $30*10^9/1.5 = 20*10^9$
No. instructions of P2 = $25*10^9/1.0 = 25*10^9$
No. instructions of P3 = $40*10^9/2.2 = 18.18*10^9$

c.

CPI_{new}=CPI_{old}*1.2, then CPI of P1 = 1.8, CPI of P2 = 1.2, CPI of P3 = 2.6.
f=No. instr.*CPI/time, then
f of P1 = $20*10^9*1.8/7$ = 5.14GHz
f of P2 = $25*10^9*1.2/7$ = 4.28GHz
f of P3 = $18.18*10^9*2.6/7$ = 6.75GHz

1.8

1.8.1.

dynamic power = $\frac{1}{2} \times C \times V^2 \times F$, then C = $\frac{2*DP}{V^2 \times F}$
Pentium 4: C = $3.2*10^{-8}$F
Core i5: C = $2.9*10^{-8}$F

1.8.2

Percentage of static power
Pentium 4: 10/100 = 10%
Core i5: 30/70 = 42.9%
Ratio of static to dynamic
Pentium 4: 10/90 = 0.11
Core i5: 30/40 = 0.75

1.8.3

P = dynamic power(DP) + static power(S)
Pentium 4:
Static power(S) = V× I, then I = 10/1.25 = 8A
$\frac{P_{new}}{P_{old}} = \frac{8 \times V_{new} + \frac{1}{2} \times C \times V_{new}^2 \times 3.6 \times 10^9}{100} = 0.9$, then $V_{new} = 1.18V$
Core i5:
Static power(S) = V× I, then I = 30/0.9 = 33.3A

$$\frac{P_{new}}{P_{old}} = \frac{33.3\times V_{new}+\frac{1}{2}\times C\times V_{new}^2\times 3.4\times 10^9}{70} = 0.9, \text{ then } V_{new} = 0.84V$$

1.9

	Arithmetic	Load / Store	Branch
CPI	1	12	5
1 processor	2560M	1280M	256M
2 processors	1830M	914M	256M
4 processors	914M	457M	256M
8 processors	457M	229M	256M

1.9.1

1 processor

Execution time

$$\frac{2560\text{M} * 1 + 1280\text{M} * 12 + 256\text{M} * 5}{2 * 10^9} = 9.6 \text{ (sec)}$$

2 processor

Execution time

$$\frac{1830\text{M} * 1 + 914\text{M} * 12 + 256\text{M} * 5}{2 * 10^9} = 7.04 \text{ (sec)}$$

Speedup

$$\frac{9.6}{7.04} = 1.36$$

4 processor

Execution time

$$\frac{914\text{M} * 1 + 457\text{M} * 12 + 256\text{M} * 5}{2 * 10^9} = 3.84 \text{ (sec)}$$

Speedup

$$\frac{9.6}{3.84} = 2.5$$

8 processor

Execution time

$$\frac{457\text{M} * 1 + 229\text{M} * 12 + 256\text{M} * 5}{2 * 10^9} = 2.23 \text{ (sec)}$$

Speedup

$$\frac{9.6}{2.23} = 4.3$$

1.9.2

1 processor

Execution time

$$\frac{2560M * 2 + 1280M * 12 + 256M * 5}{2 * 10^9} = 10.88 \ (sec)$$

2 processor

Execution time

$$\frac{1830M * 2 + 914M * 12 + 256M * 5}{2 * 10^9} = 7.954 \ (sec)$$

4 processor

Execution time

$$\frac{914M * 2 + 457M * 12 + 256M * 5}{2 * 10^9} = 4.296 \ (sec)$$

8 processor

Execution time

$$\frac{457M * 2 + 229M * 12 + 256M * 5}{2 * 10^9} = 2.471 \ (sec)$$

1.9.3

$$\frac{2560M * 1 + 1280M * CPI + 256M * 5}{2 * 10^9} = 3.84 \ (sec)$$

$$CPI = 3$$

1.11.1

CPI = clock rate × CPU time/instr. count
clock rate = 1/cycle time = 3 GHz
CPI(bzip2) = 3 × 10^9× 750/(2389 × 10^9) = 0.94

1.11.2

SPEC ratio = ref. time/execution time
SPEC ratio(bzip2) = 9650/750 = 12.86

1.11.3

CPU time = No. instr. × CPI/clock rate
If CPI and clock rate do not change, the CPU time increase is equal to the increase in the number of instructions, that is 10%.

1.11.4

CPU time(before) = No. instr. × CPI/clock rate
CPU time(aft er) = 1.1 × No. instr. × 1.05 × CPI/clock rate
CPU time(aft er)/CPU time(before) = 1.1 × 1.05 = 1.155. Thus, CPU time is increased by 15.5%.

1.11.5

SPECratio = reference time/CPU time
SPECratio(aft er)/SPECratio(before) = CPU time(before)/CPU time(aft er) = 1/1.1555 = 0.86. The SPECratio is decreased by 14%.

1.11.6

CPI = (CPU time × clock rate)/No. instr.
CPI = 700 × 4 × 10^9/(0.85 × 2389 × 10^9) = 1.37

1.11.7

Clock rate ratio = 4 GHz/3 GHz = 1.33
CPI @ 4 GHz = 1.37, CPI @ 3 GHz = 0.94, ratio = 1.45
They are diff erent because, although the number of instructions has been reduced by 15%, the CPU time has been reduced by a lower percentage.

1.11.8

700/750 = 0.933. CPU time reduction: 6.7%

1.11.9

No. instr. = CPU time × clock rate/CPI
No. instr. = 960 × 0.9 × 4 × 10^9/1.61 = 2146 × 10^9

1.11.10

Clock rate = No. instr. × CPI/CPU time.
Clock rate new = No. instr. × CPI/0.9 × CPU time = 1/0.9 clock rate old = 3.33 GHz

1.11.11

Clock rate = No. instr. × CPI/CPU time.
Clock rate new = No. instr. × 0.85 × CPI/0.80 CPU time = 0.85/0.80, clock rate old = 3.18 GHz

1.13

1.13.1 T_{fp} = 70 × 0.8 = 56 s. T_{new} = 56 + 85 + 55 + 40 = 236 s.
Reduction = 1-236/250 = 5.6%

1.13.2 T_{new} = 250 × 0.8 = 200 s, $T_{fp} + T_{l/s} + T_{branch}$ = 85+70+40 = 195s, T_{int} = 55s → 5s. Reduction time INT = 1 - 5/55 = 90.9%

1.13.3 T_{new} = 250 × 0.8 = 200 s, $T_{fp} + T_{int} + T_{l/s}$ = 210 s. NO

1.14

1.14.1 Clock cycles = CPI_{fp} × No. FP instr. + CPI_{int} × No. INT instr. + $CPI_{l/s}$ × No. L/S instr. + CPI_{branch} × No. branch instr.
T_{CPU} = clock cycles/clock rate = clock cycles/2 × 10^9
clock cycles = 512 × 10^6
T_{CPU} = 0.256 s

To have the number of clock cycles by improving the CPI of FP instructions:

$CPI_{improved\ fp}$ × No. FP instr. + CPI_{int} × No. INT instr. + $CPI_{l/s}$ × No. L/S instr. + CPI_{branch} × No. branch instr. = clock cycles/2

$CPI_{improved\ fp}$ = (256 − 462)/50 < 0 = = > not possible

1.14.2 Using the clock cycle data from 1.14.1.

To have the number of clock cycles improving the CPI of L/S

CPI_{fp} × No. FP instr. + CPI_{int} × No. INT instr. + $CPI_{improved\ l/s}$ × No. L/S instr. + CPI_{branch} × No. branch instr. = clock cycles/2

CPI improved l/s = (256 − 192)/80 = 0.8

1.14.3 CPI_{int} = 0.6 × 1 = 0.6; CPI_{fp} = 0.6 × 1 = 0.6; $CPI_{l/s}$ = 0.7 × 4 = 2.8; CPI_{branch} =0.7 × 2 = 1.4

T_{CPU} (before improv.) = 0.256 s; T_{CPU} (after improv.) = 0.171 s

1.15

processors	exec time/processor	time w/ overhead	speedup	actual/ideal
1	100			
2	50	54	1.85	92.6%
4	25	29	3.45	86.2%
8	12.5	16.5	6.06	75.8%
16	6.25	10.25	9.76	61.0%
32	3.125	7.125	14.04	43.9%
64	1.5625	5.5625	17.98	28.1%
128	0.78125	4.78125	20.92	16.3%