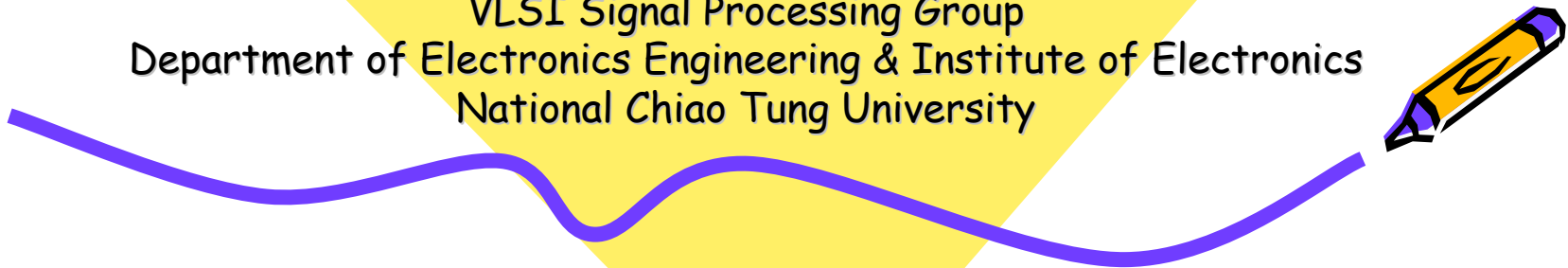# 5014: Computer Architecture

## Chih-Wei Liu

### VLSI Signal Processing Group
Department of Electronics Engineering & Institute of Electronics
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# Course Information

- Lecture:
  - Chih-Wei Liu 劉志尉
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    - 5731685, ED618
- Teaching Assistants:
  - 歐士豪 shou@twins.EE.NCTU.edu.tw
  - 陳信凱 skchen@twins.ee.nctu.edu.tw
  - 54225, ED412

# Course Information

- Text
  - J. L. Hennessy and D.A. Patterson, *Computer Architecture: A Quantitative Approach*, 4th Edition, Morgan Kaufmann Publishers, 2007
- One semester course, which might include Chapters 1~5, Appendix A~C
- Prerequisites:
  - Computer organization
  - Computer programming

# Processor Performance



vs. VAX 11/780, as measured by the SPECint benchmark
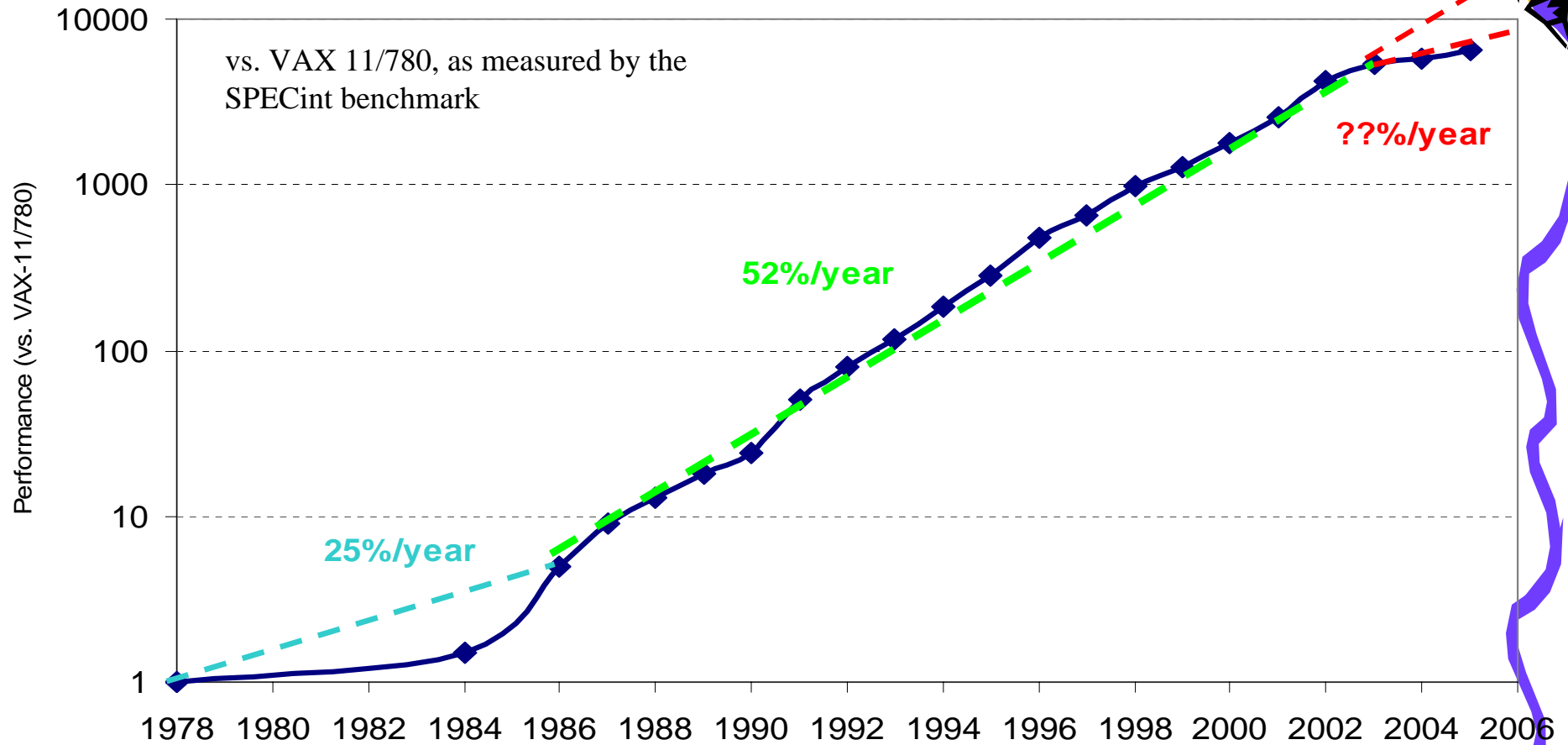
**??%/year**

**52%/year**

**25%/year**

- **VAX         : ~25%/year 1978 to 1986**
- **RISC + x86: ~52%/year 1986 to 2002**

4

# Textbook Structure

- ILP (Instruction-Level Parallelism)
  - Appendix A, Chapters 2&3, and Appendices F&G

- Memory Hierarchy
  - Appendix C and Chapters 5&6

- TLP (Thread-Level Parallelism), DLP (Data-Level Parallelism)
  - Chapter 4, Appendices H& E

- ISA (Instruction Set Architecture)
  - Appendices B&J

# About the Textbook

- **Crosscutting Issues** section
  - A feature that shows how the ideas covered in one chapter intersect with those given in other chapters

- **Putting It All Together** section
  - To show and how the ideas in crosscutting issues section are used in a real machine

- **Another View** section
  - A new feature for the 3rd Ed. that gives a real-world example from the embedded or server space

- **Fallacies and Pitfalls** section
  - This help the reader to learn from the mistakes and traps of others.

# Course Grade (tentative)

- Lectures and Homeworks 15%

  - Adapted from Prof. David Patterson's class notes

  - Please avoid arriving late or leaving early.

  - At least one problem sets with respect to each lecture

  - Homework should be handed in on time

- Project 25%

- Midterm and Final Exams. 60%

- (Extra points 5%)

# Spring 2010 Outline

- Chap. 1 Fundamentals of Computer Design
  - The quantitative approach and performance measurement

- Appendix B Instruction Set Principles and Example (Reading)
  - Examples of contemporary and important historical ISA

- Appendix A Pipelining (Reading)
- Chap. 2 Instruction-Level Parallelism and its Exploitation
- Chap. 3 Limits on Instruction-Level Parallelism
  - To execute more than one instruction at a time
  - The complexity grows $\sim N^2$ in order to execute N instructions simultaneously

- Chap. 4 Multiprocessors and Thread-Level Parallelism
  - A key to simple, power-efficient, and high-performance system implementation that avoids the $N^2$ problem
  - Shared-memory architectures, Sun T1 (Niagara) processor: 32 threads on a chip

- Appendix C Review of Memory Hierarchy
- Chap. 5 Memory Hierarchy Design
  - Cache and memory hierarchies and virtual memory

# Project

- Task/Thread Management on Multi-core System
  - LAB1: MIPS-compatible IMP DSP
  - LAB2: Profiling, Partitioning, and IPC Overhead
  - LAB3: Task/Thread Management

- Operate Your Graphic Card
  - LAB1: nVidia GeForce Graphic Card
  - LAB2: Tradeoff between ILP and TLP
  - LAB3: Optimization for NUMA memory access